CX25800
PCI Video Decoder with Mono Audio Input

Data Sheet

DSH-201233A
July 2007

CONEXANT

Ordering Information

Model Number	Description	Package	Operating Temperature	Minimum Order Quantities
CX25800		176-pin LQFP	0 to +70 ^{0}C	

Revision History

Revision	Date	Description
A	July 2, 2007	Initial Release

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Preliminary Information

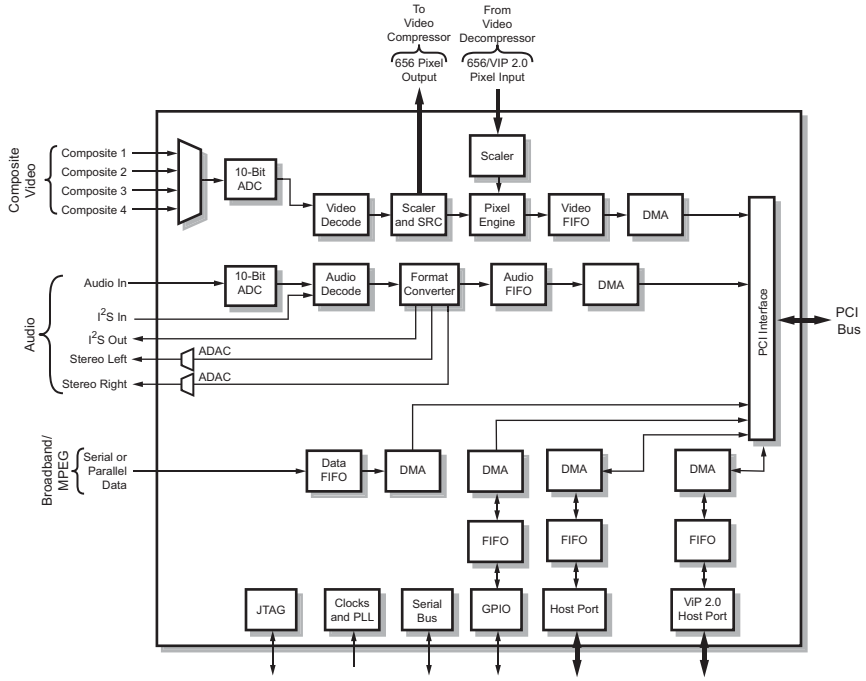
This document contains information on a new product. The parametric information, although not fully characterized, is the result of testing initial devices.

CX25800

PCI Video Decoder with Mono Audio Input

The CX25800 is a highly flexible single chip solution that enables video and audio capture over a PCI bus. Designed for surveillance applications, the CX25800 accepts analog NTSC and PAL video from cameras, as well as line-level mono audio inputs from microphones. The CX25800 enables audio/video capture and playback on PC-based Digital Video Recorders (DVRs). The CX25800 also supports a variety of peripheral connectivity options via its GPIO pins, BT.656, I^2S, MPEG port, and host port interfaces.

Functional Block Diagram



Distinguishing Features

Video Subsystem

- 10-bit video ADCs
- NTSC and PAL Composite video formats
- Capture resolution up to 720x576 (Square Pixel PAL)
- NTSC and PAL adaptive comb filter for 2-D Y/C luminance and chrominance separation
- AGC video circuit
- Multiple YCrCb and RGB pixel formats and YUV planar formats support on output
- Selectable pixel density: 16 and 24 bits per pixel
- Complex clipping of video source and VGA video overlay
- Allowance for different program control and color space/scaling for even and odd fields
- Support of Windows “Scatter/ Gather” DMA
- High-quality multitap horizontal and vertical image scaler for decoded video or 4:2:2 sources
- ITU-R BT.656 8-bit or 10-bit 4:2:2 output port
- ITU-R BT.656/VIP 2.0 pixel input port
- Flexible VBI data capture for closed captioning, teletext, and other analog data types
- Hue, brightness, contrast, saturation control for video decoder

(Continued on the next page)

Distinguishing Features (continued)

Audio Subsystem

- 10-bit A/D for mono analog audio input
- Decoded 48 kHz audio stream to PCI bus for real time encoding to MP3
- Integrated 90 dB SNR stereo audio DACs to drive sound card or headphones
- I^2S input port for external source connectivity to on-board stereo DACs
- I^2S output port to drive coaxial/ optical digital audio interface
- Flexible audio sample rate converter

Multipurpose I/O Subsystem

- Bidirectional 33 MBps VIP 2.0 Host port
- Bidirectional 10 MBps Intel/ Motorola-compatible General Purpose Host port
- Unidirectional 10 MBps parallel/ serial MPEG Transport/Data Stream port- compatible with all Conexant digital television channel demodulator ICs.
- MPEG Packet Synchronization
- User-defined General Purpose Input/Output pins

PCI Subsystem

- 5 independent functions each with Target/Master and Local register space (Video, Audio, MPEG Port, VIP 2.0 Host Port, GP Host Port)
- All RISC/Control programs executed on-chip
- On-chip SRAM for PCI data buffering Up/Down
- Vital product data
- DMA byte alignment
- PCI revision 2.3-compliant

Miscellaneous

- ACPI and power-down support
- Only one crystal for all video and audio decoding required
- 400 kHz serial bus master
- JTAG boundary scan interface
- Compact 176-pin LQFP

Applications

- Surveillance camera systems

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1 Product Overview

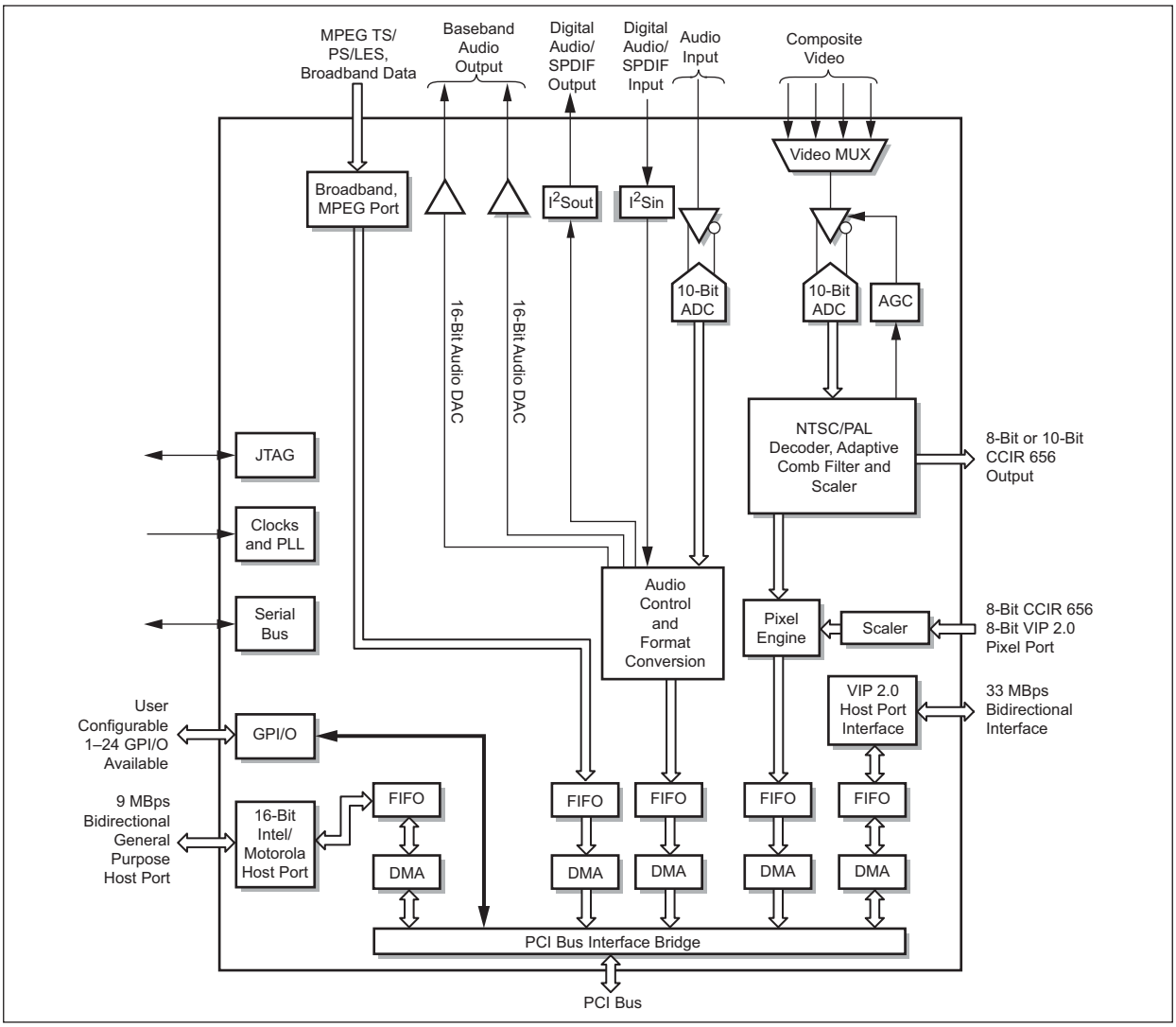
1.1 Functional Overview

The CX25800 is implemented as a multifunction PCI bus master and fabricated in an advanced CMOS process operating from +3.3 V I/P and 1.8 V (digital core) power supplies. PCI inputs are +5 V and 3.3 V tolerant.

The CX25800 is designed to enable high-functionality broadcast- centric PC cards that require high speed Input/Output (I/O) capability. This capability is necessary to support simultaneous compressed and uncompressed digital video/audio data flows in conjunction with hardware MPEG II/MPEG IV encoders and decoders.

Figure 1 illustrates a block diagram of the CX25800.

Figure 1. CX25800 Detailed Block Diagram



1.2 Detailed Features

1.2.1 Analog Video Capture

1.2.1.1 Overview

The CX25800 integrates a 10-bit NTSC/PAL composite video decoder, image resizer/scaler, Direct Memory Access (DMA) controller, and Peripheral Component Interface (PCI) Bus master on a single device. The CX25800 can place video data directly into host memory for video capture applications and into a target video display frame buffer for video overlay applications. As a PCI initiator, the CX25800 can take control of the PCI bus as soon as it is available, thereby avoiding the need for onboard frame buffers. The CX25800 contains a pixel data First In, First Out (FIFO) to decouple the high-speed PCI bus from the continuous video data stream. The video data input can be scaled, color-translated, and burst-transferred to a target location on a field basis.

1.2.1.2 Input Interface

Analog video signals are input to the CX25800 through a four-input multiplexer. An Automatic Gain Control (AGC) circuit enables the CX25800 to compensate for nonstandard amplitudes in the analog signal input.

1.2.1.3 Image Scaler

The CX25800 can reduce the video image size in both horizontal and vertical directions independently, using arbitrarily selected scaling ratios. The X and Y dimensions can be scaled down to one-sixteenth of the full resolution. Horizontal scaling is implemented with a six-tap interpolation filter, while up to five-tap interpolation is used for vertical scaling with a line store. The video image can be arbitrarily cropped by reducing the number of active scan lines and active horizontal pixels per line. The CX25800 supports a temporal decimation feature that reduces video bandwidth. This is accomplished by allowing frames or fields to be dropped from a video sequence at fixed but arbitrarily selected intervals.

1.2.1.4 Reduced Instruction Set Computer Engine

The CX25800 enables separate destinations for the odd and even video fields, each controlled by a pixel Reduced Instruction Set Computer (RISC) instruction list. This instruction list is created by the CX25800 device driver and can be run in the onboard memory or host memory. The instructions control the transfer of pixels to target memory locations on a byte resolution basis. Complex clipping can be accomplished by the instruction list, blocking the generation of PCI bus cycles for pixels that are not to be seen on the display.

The DMA channels can be programmed on a field basis to deliver the video data in packed or planar format. In packed mode, YCrCb data is stored in a single continuous block of memory. In planar mode, the YCrCb data is separated into three streams which are burst to different target memory blocks. Having the video data in planar format is useful for applications where the data compression is accomplished through software and the CPU.

1.2.1.5 UltraLock™

The CX25800 employs a proprietary technique known as UltraLock to lock to the incoming analog video signal. It always generates the required number of pixels per line from an analog source in which line length can vary by as much as a few microseconds. UltraLock's digital locking circuitry enables the CX25800 to lock onto video signals quickly and accurately, regardless of their source. Because the technique is completely digital, UltraLock can recognize unstable signals caused by VCR head switches or any other deviation and adapt the locking mechanism to accommodate the source. UltraLock uses nonlinear techniques that are difficult, if not impossible, to implement in genlock systems. And, unlike linear techniques, it adapts the locking mechanism automatically.

1.2.1.6 Vertical Blanking Interval (VBI) Data Capture

The CX25800 provides a flexible solution for capturing and decoding disparate VBI data types such as closed caption data, teletext, Vertical Internal Time and Control (VITC) codes, HTML data, or multicast data. The CX25800 can operate in a VBI Line Output mode, in which the VBI data is only captured during selected lines. This mode of operation enables concurrent capture of VBI lines containing ancillary data and normal video image data. In addition, the CX25800 supports a VBI Frame Output mode in which every line in the video frame is treated as if it were a VBI line. This mode of operation is designed for use with still-frame capture and processing applications where sophisticated image decoding can be performed in the software domain.

1.2.2 Analog Audio Capture

The CX25800 captures mono analog audio. The decoded audio is sample-rate converted to a 48-kHz Pulse Code Modulation (PCM) signal to simplify processing and interfacing. This 48-kHz stream can be routed to the built-in +85 dB Signal-to-Noise Ratio (SNR) stereo audio Digital-to-Analog Converters (DACs) for connection to the PC's sound card or headphones, to an external digital-audio interface, or to the PCI bus and host for direct capture by a software audio codec.

If capture of line-level stereo audio signals is required, an inexpensive audio Analog-to-Digital Converter (ADC) can be directly connected to the CX25800's I^2S input port and controlled through the serial bus master.

1.2.3 ITU-R 656 4:2:2 Data Output

The CX25800 provides a 27-MHz, 8- or 10-bit ITU-R 656 decoded video output interface to allow connection of a third-party MPEG II encoder or other type of video codec. This is useful when the host CPU is not powerful enough to perform such tasks in software, or when high-quality encoding must be achieved.

1.2.4 ITU-R 656/VIP 2.0 Pixel Data Input

The CX25800 provides a 27-MHz, 8-bit ITU-R 656 decoded video input interface. This allows a third-party MPEG II decoder or codec to send 4:2:2 data over the PCI bus to a target video display frame buffer for video overlay.

1.2.5 MPEG Data Port

Channel demodulators used for digital television or broadband data applications over terrestrial, satellite, or cable networks can be directly connected to the CX25800's MPEG data port. As a result, transport streams can be delivered to the host for subsequent storage to disk or software decode. Either parallel, common-interface Digital Video Broadcasting (DVB) or serial data paths from the channel demodulator can be supported at data transfer rates of up to 80 Mbps. If the serial interface mode is used, the remaining unused pins on this port can be allocated as General Purpose Input/Output (GPIO).

1.2.6 General Purpose Host Interface Port

The General Purpose Host interface allows connection of moderate-to-relatively slow-speed, third party peripherals such as infrared remote control processors, codec host ports, smart card controllers (etc.). This port allows simultaneous connection to two peripherals gluelessly, or to as many as four peripherals with the use of external glue logic to provide the additional chip selects. This interface can have one upstream and one downstream DMA channel active to or from the external peripherals at any given time. Data bursting is not supported.

1.2.7 GPIO Port

The CX25800 provides up to 24 GPIO pins. These GPIO pins are shared with the following pins/ports groups so that the user can determine exactly which pins can be dedicated to specific functions versus general purpose I/O functions.

1. MPEG Parallel Data Port
2. ITU–R 656 4:2:2 Data Output
3. ITU–R 656 4:2:2 Data Input
4. Extended VIP Host Port
5. Extended General Purpose Host Port (GPHP)

1.2.8 Serial Bus Interface

The CX25800's serial bus interface supports both 99.2-kHz timing transactions and 396.8-kHz, repeated start, multibyte sequential transactions. As a serial bus master, the CX25800 can program other devices on the video card, such as MUXs, as long as the device address is known. The CX25800 supports multibyte sequential reads (more than one transaction) and multibyte write transactions (greater than three transactions), which enable communication to devices that support auto-incremental internal addressing.

1.2.9 PCI Bus Interface

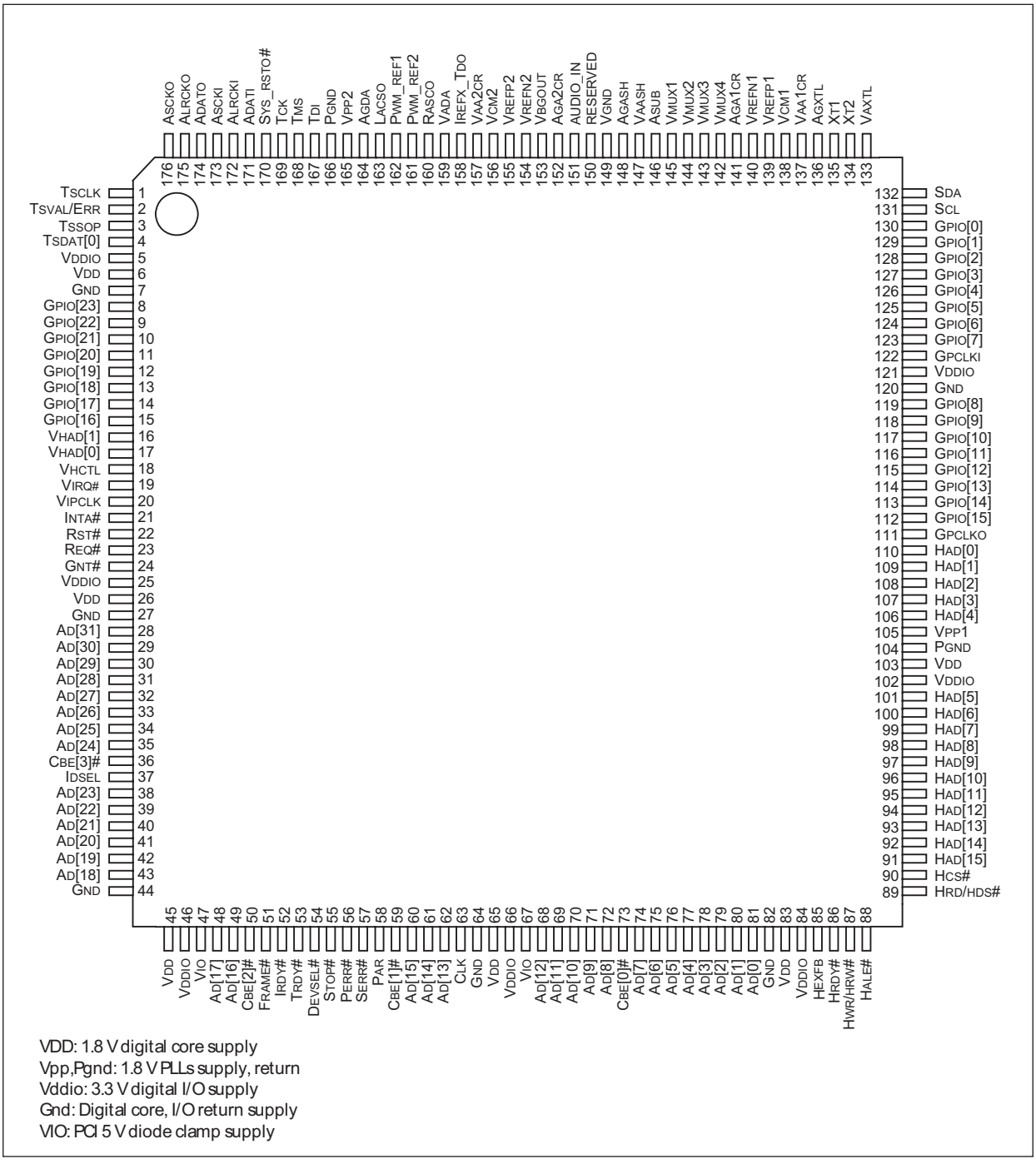
The CX25800 is designed to efficiently utilize the available 132 MBps PCI bus. The 32-bit dwords are output on the PCI bus with the appropriate image data under the control of the DMA channels. The video stream consumes bus bandwidth with average data rates varying from 44 MBps for full-size 768 576 PAL RGB32, to 4.6 MBps for NTSC CIF 320 240 RGB16, to 0.14 MBps for NTSC ICON 80 60 8-bit mode.

The pixel instruction stream for the DMA channels consumes a minimum of 0.1 MBps. The CX25800 provides the means for mitigating bandwidth bottlenecks caused by slow targets and long bus access latencies that can occur in some system configurations. To overcome these system bottlenecks, the CX25800 gracefully degrades and recovers from FIFO overruns to the nearest pixel in real time.

1.3 Pin Descriptions

Figure 2 displays the CX25800 pinout diagram. Table 1 provides a description of pin functions grouped by common function.

Figure 2. CX25800 Pinout Diagram



VDD: 1.8 V digital core supply
Vpp,Pgnd: 1.8 V PLLs supply, return
Vddio: 3.3 V digital I/O supply
Gnd: Digital core, I/O return supply
VIO: PCI 5 V diode clamp supply

Table 1. Pin Descriptions Grouped by Pin Function (1 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description
PCI Interface (50 Pins)					
63	CLK	I	—	Clock	All PCI signals except RST# and INTA# are sampled on the rising edge of this 33.3333 MHz clock.
22	RST#	I	—	Reset	Bus reset causes all PCI outputs to asynchronously three-state.
23	REQ#	O	t/s	Request	Agent requests bus.
24	GNT#	I	—	Grant	Agent grants bus.
37	IDSEL	I	—	Initialization Device Select	Selects device during configuration read and write transactions.
[28–35, 38–43, 48, 49, 60–62, 68–72, 74–81]	AD[31:0]	I/O	t/s	Address/Data	Address phase when FRAME# is 1st asserted, and data transfer when IRDY# and TRDY# are both asserted.
[36, 50, 59, 73]	CBE[3:0]#	I/O	t/s	Bus Command/ Byte Enables	Bus transaction-type command during address phase, and byte enables during entire data phase.
58	PAR	I/O	t/s	Parity	Even parity across {AD, C/BE#}, lags address/data phase
51	FRAME#	I/O	s/t/s	Cycle Frame	Asserted to begin bus transaction. Deasserted when transaction in final data phase.
52	IRDY#	I/O	s/t/s	Initiator Ready	Indicates the initiator is ready to accept read data or has placed valid write data on the AD.
53	TRDY#	I/O	s/t/s	Target Ready	Indicates the target is ready to accept write data or has presented valid data on AD during a read.
54	DEVSEL#	I/O	s/t/s	Device Select	Indicates the driving device has decoded the address as the target of the current access.
55	STOP#	I/O	s/t/s	Stop	Target requesting master to stop current transaction.
56	PERR#	I/O	s/t/s	Parity Error	Report data parity error.
57	SERR#	O	t/s	System Error	Report address parity or system error.
21	INTA#	O	t/s	Interrupt A	Request an interrupt.
JTAG Signals (4 Pins)					

Table 1. Pin Descriptions Grouped by Pin Function (2 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description
169	TCK	I	—	Test Clock	Used to synchronize all JTAG test structures. Tie low when not using JTAG.
168	TMS	I	r	Test Mode Select	Transitions drive JTAG state machine sequence. Tie high or leave floating when not using JTAG. A fixed sequence on this pin initializes the JTAG tap controller.
167	TDI	I	r	Test Data In	Load input instructions and/or test vector data for boundary scan and internal scan. Tie high or leave floating when not using JTAG.
158	IREFX—TDO	O		Test Data Out	Output for verifying JTAG serial operations. The output is three-stated when not using JTAG port.
VIP 2.0 Host Master Signals (5 or 11 Pins)					
16, 17 8–15	VHAD[1:0](1) GPIO[23:16]	I/O	—	VIP Host Address/ Data	VIP Address and Data bus, defaults to VIP1.1 interface with 2 addr/data pins. Can be configured as VIP 2.0 with 8 address/ data pins (GPIO).
18	VHCTL	I/O	—	VIP Host Control	VIP System Host control
19	VIRQ#	I/O	od	VIP Interrupt Request	VIP Interrupt Request (open drain)
20	VIPCLK	O	—	VIP Clock	VIP master output clock. This clock is buffered. PCI CLK = 33.3333 MHz.
Transport Stream Signals (4 or 11 Pins)					
4	TSDAT[0](2)	I	—	Transport Stream Data	Transport Stream Input data bus. TSDAT[0] is used in serial mode.
3	TSSOP	I	—	Transport Stream Start of Packet	Transport Stream Start-of-Packet indicator. Indicates first byte in serial or parallel transport packet.
2	TSVAL/ERR	I	—	Transport Stream Error/Valid	Transport Stream Error or Valid indicator
1	TSCLK	I	—	Transport Stream Clock	Transport Stream input clock. All other transport stream inputs are sampled on the rising (falling) edge of TSCLK.
Host Master Signals (22 Pins)					
[91–101, 106–110]	HAD[15:0]	I/O	—	General Purpose Host Address/Data	Bidirectional address/data access bus
90	HCS#	O	—	General Purpose Host Chip Select	External chip select

Table 1. Pin Descriptions Grouped by Pin Function (3 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description
89	HRD#/ HDS#	O	—	General Purpose Host Read/Data Strobe	Either the active-low read signal or the programmable polarity data strobe signal
88	HALE#	O	—	General Purpose Host Address Latch Enable	Address Latch Enable signal, used only in multiplexed 16-bit address/data mode
87	HWR/ HRW#	O	—	General Purpose Host Write/Read, not Write	Either the active-low write signal or the read/write bar
86	HRDY#	I	r	General Purpose Host Ready	External data transfer acknowledge signal
85	HEXFB	I	r	General Purpose Host External Status	Handshaking signal for use in DMA mode to indicate the status of the external source or destination FIFO.
GPIO/Serial Bus/Reset (29 Pins)					
[8–15, 112–119, 123–130]	GPIO[23:0]	I/O	I/O	GPIO	See GPIO Cross-Reference Table.
122	GPCLKI	I	I	General Purpose Input Clock	Digital Video Input Reference clock
111	GPCLKO	O	O	General Purpose Output Clock	Digital Video Output Reference clock
132	SID	I/O	od	Serial Data	Bit data or acknowledge
131	SIC	I/O	od	Serial Clock	Bit clock
170	SYS_RSTO#	O	t/s	System Reset Out	Logical PCI reset, soft reset, or power-on reset output. This is used to reset CX25800's peripheral under software control or with hard reset.
Digital Audio (6 Pins)					
171	ADATI	I	r	Audio Data In	Bit Serial Input data
172	ALRCKI	I	r	Audio Left/Right Clock In	Left/Right Framing Input clock
173	ASCKI	I	r	Audio Serial Clock Input	Bit Serial Input clock
174	ADATO	O	r	Audio Data Out	Bit Serial Output data
175	ALRCKO	O	r	Audio Left/Right Clock Out	Left/Right Framing Output clock

Table 1. Pin Descriptions Grouped by Pin Function (4 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description
176	ASCKO	O	r	Audio Serial Clock Output	Bit Serial Output clock
Crystal Interface Signals (4 Pins)					
134	XT2	O	—	XT2	Crystal oscillator pin
135	XT1	I	—	XT1	Crystal oscillator or clock oscillator input pin can be connected to XT1.
133	VAXTL	—	—	PSUP_XTAL	XTAL and Sample and Hold digital power/ ground. Nominal VA = 3.3 V.
136	AGXTL	—	—	NSPU_XTAL	
ADC Interface (23 Pins)					
[145:142]	VMUX[1:4]	I	A	Video Mux {1:4}	Analog composite video inputs to the on-chip 4:1 analog multiplexer. Leave unused inputs No Connect. Grounding unused inputs may draw excessive power.
150	Reserved				Leave this pin No Connect
151	AUDIO IN	I	A	Audio IN	Analog audio input. Leave unused input No Connect or connected to ground via a decoupling capacitor. Grounding this input may draw excessive power.
138 156	VCM1 VCM2	O	A	VCM_ADC{1:2}	Common mode voltage reference
140 154	VREFN1 VREFN2	O	A	VREFN{1:2}	Input Negative reference (1.0 V)—one for each Y and C/Aud ADCs, cap to AGA.
139 155	VREFP1 VREFP2	O	A	VREFP{1:2}	Input Positive reference (1.8 V)—one for each Y and C/Aud ADCs, cap to AGA.
153	VBGOUT	O	A	VBGOUT	Voltage reference 1.21 V nominal, cap to AGA.
137, 157	VAA{1:2}CR	—	A	VAA{1:2}CR	A/D core power/ground. Nominal VA = 3.3 V
141, 152	AGA{1:2}CR	—	A	AGA{1:2}CR	
146	ASUB	—	—	ASUB	A/D core substrate (ground)
147	VAASH	—	—	PSUPA_SHA_ADC	A/D Sample and Hold Analog power/ ground. Nominal VA = 3.3 V.
148	AGASH	—	—	NSUPA_SHA_ADC	

Table 1. Pin Descriptions Grouped by Pin Function (5 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description
149	VGND	I	A/D	Virtual Ground	Single-end-to-differential converter input for common-mode noise rejection. Connect to analog ground through 3.3 μF series capacitor.
105, 165	VPP1/VPP2	—	—	VPP1, VPP2	PLL power supply. VD = 1.8 V.
104, 166	PGND	—	—	PGND	PLL return supply
158	IREFX_TDO	I/O	A/D	IREF_EXT/TDO	Shared analog current ref pin JTAG TDO pin
Audio Output DAC Signals (6 Pins)					
159	VADA	—	—	VADA	DAC analog core power and ground. VA = 3.3 V
164	AGDA	—	—	AGDA	
163	LASCO	O	A	LASCO	DAC Pulse Width Modulator (PWM), left stereo audio output channel
160	RASCO	O	A	RASCO	DAC PWM, right stereo audio output channel
161	PWM_REF2	O	A	PWM_REF2	Audio DAC reference, right
162	PWM_REF1	O	A	PWM_REF1	Audio DAC reference, left
I/O and Core Power and Ground (23 Pins)					
6, 26, 45, 65, 83, 103	VDD	—	—	VDD	Digital core power supply. Nominal VDD = 1.8 V.
7, 27, 44, 64, 82, 120	GND	—	—	GND	Ground for digital core (GND)
5, 25, 46, 66, 84, 102, 121	VDDIO	—	—	VDDI and VDDO	Digital inputs/outputs power supply. VD = 3.3 V.
47, 67	VIO	—	—	VIO	+5 V reference for 5 V-tolerant PCI input buffers

Table 1. Pin Descriptions Grouped by Pin Function (6 of 6)

Pin Number	Pin Name	Dir	Type	Signal	Description

FOOTNOTES:

(1) VHAD[1:0] is the default for the 5-pin VIP Host Port setting.

(2) TSDAT[0] is the default for the 4-pin serial MPEG Data Port setting. The 11-pin setting shares GPIO pins.

GENERAL NOTES:

1. Type:ractive resistive pull-up
   od: open-drain
   t/s: three-state
   s/t/s: sustained three-state
   [x:y]: Bus
   {u:v:}Array of signal ports—expand to number without braces.
2. All signal I/O are LVTTL compatible (3.3 V operation with 3.9 V tolerance), except for the PCI signals which are all 5.5 V tolerant.
3. All inputs are Schmitt unless otherwise noted. The PCI inputs do not have hysteresis.
4. All outputs have drive capability I_{OL} = 4 mA unless otherwise noted.

2 Functional Description

2.1 Audio Input

This section describes the functionality of the analog audio input. The following paragraphs define the logical sequence, from the audio input at the analog front end, to the output of digital audio samples, to the PCI bus or on-board DACs.

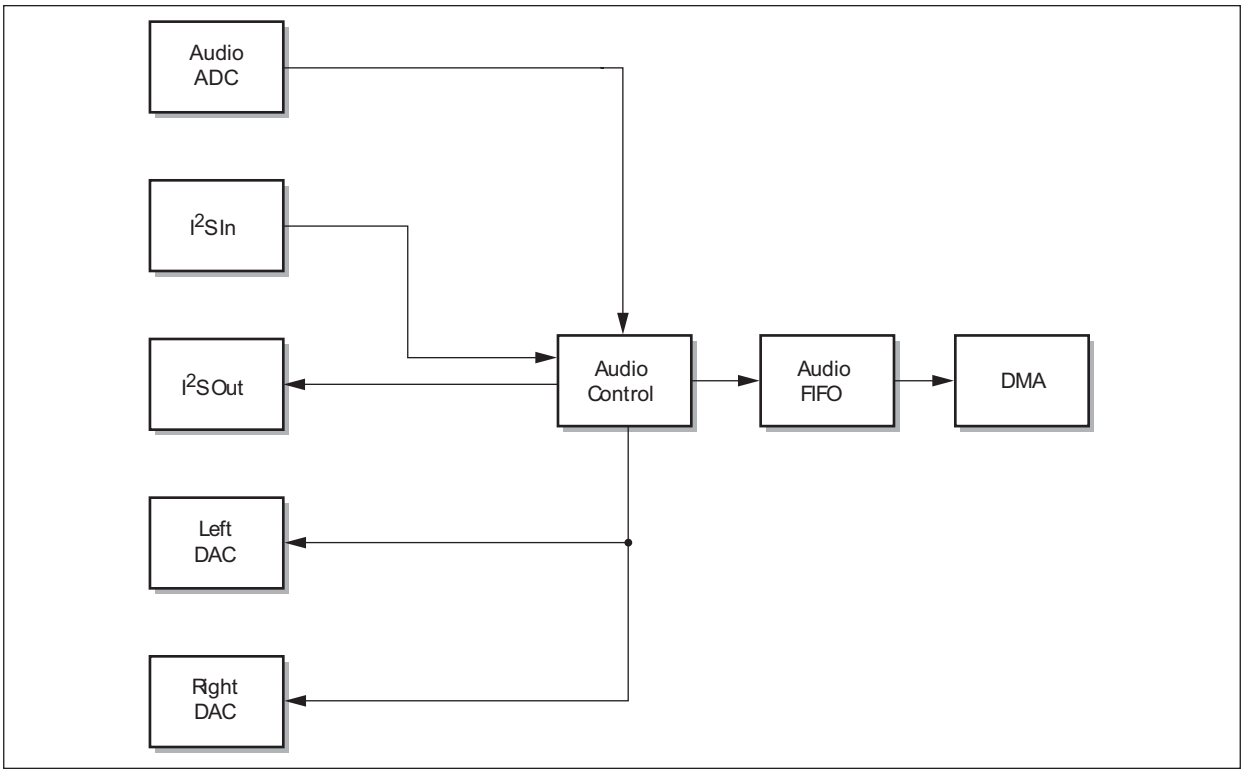
2.1.1 Overview

Analog audio input can be output directly to the on-board DACs for connection to the PC's sound card, to I^2S for high-fidelity digital coaxial and optical interfaces, or to the host for software-based playback or encoding.

The major functional blocks of the audio subsystem are illustrated in Simplified Block Diagram of CX25800 Audio Subsystem and are broken down into the following sections:

- Audio-ADC
- Audio PLL initialization
- Input source select
- Dematrix control
- Audio control and Sample Rate Converter
- I^2S input and output
- Audio DACs

Figure 3. Simplified Block Diagram of CX25800 Audio Subsystem



2.1.2 Analog Input ADC

The CX2500's Audio input (pin 151) is used for sampling line level audio signals from an amplified microphone.

2.1.3 Audio PLL Initialization

The audio PLL is automatically configured for 28.636363-MHz crystal frequency with the AUD_INIT_LD register. If using a crystal of frequency other than 28.636363 MHz, please contact Conexant Applications Engineering. If using the I^2S output mode, the PLL must be programmed to exactly 221.184 MHz in fractional mode.

2.1.4 Input Source Select

The 12 LSBs [11:0] of the AUD_CTL register (location 24'h32058C) determine the desired operation of the audio decoder.

24'h32058C—AUD_CTL Register

Bits	Type	Default	Name	Description
[5:0]	RW	6'h00	Reserved	Reserved
[6]	RW	1'b0	Reserved	Reserved
[8:7]	RW	2'h0	Reserved	Reserved
[9]	RW	Reserved	Reserved	Reserved
[10]	RW	1'b0	Reserved	Reserved
[11]	RW	1'b0	Reserved	Reserved
[12]	RW	1'b0	DAC_ENABLE	DAC enable bit
[13]	RW	1'b0	I^2SOUT_ENABLE	I^2S output enable bit
[14]	RW	1'b0	I^2S_STR2DAC	I^2S input straight to DAC enable bit
[15]	RW	1'b0	I^2SIN_ENABLE	I^2S input enable bit

2.1.5 Audio Control and Sample Rate Converter

2.1.5.1 Audio Demodulator Sample Rate Converter

Audio formats supported by the CX25800 are upconverted from their native sampled format to 48 kHz. This simplifies internal filtering and interfacing to external hardware peripherals through I^2S, the internal audio DACs, or to software codecs.

2.1.5.2 Volume

The volume control provides gain to both the left and right audio channel in 1 dB increments. The volume range is –63 to 0 dB and is controlled by the VOL_CTL register.

In addition, flexible control over muting is possible by the ability to control the muting of the selected source from the audio demodulator, the I^2S output, and the audio DAC. During initialization, from reset to the end of the AUD_START_TIMER count, all three of these mutes are enabled automatically to avoid pops or clicks on any of the outputs.

24'h320594—VOL_CTL Register

Bits	Type	Default	Name	Description
[5:0]	RW	8'h00	VOLUME	Volume control in dB steps, 0 to –63 dB
[6]	RW	1'b0	SRC_MUTE_EN	Source mute enable
[7]	RW	1'b0	I^2S_MUTE_EN	I^2S mute enable
[8]	RW	1'b0	DAC_MUTE_EN	DAC mute enable
[15:9]	RW	7'h00	—	Reserved

2.1.5.3 Balance

The DAC output level can be adjusted. Digital balance control is used to alter the relative gain between the left and right channel outputs. Balance is controlled by providing an attenuation to one channel while maintaining 0 dB gain to the other channel. Attenuation of either channel is in the range of -63 to 0 dB in 1 dB steps. Balance attenuation is performed prior to the volume control. Stereo is only available via I^2S input. The analog audio input is monophonic.

24'h320598—BAL_CTL Register

Bits	Type	Default	Name	Description
[5:0]	RW	8'h00	BAL_LEVEL	Attenuation to be provided to the selected channel in dB. Range is 0 to –63 dB.
[6]	RW	1'b0	BAL_RIGHT	Select right channel for balance control if 1, select left channel if 0.
[15:7]	RO	7'h00	—	Reserved

2.1.6 I²S Input and Output

2.1.6.1 I²S Input

The CX8500 supports I²S input and output interfaces to a wide variety of external audio components. The three pins that make up the I²S input interface are ADATAI (Audio Data In, pin 171), ALRCKI (Audio Left/Right Clock In, pin 172), ASCKI (Audio Serial Clock In, pin 173).

The I²S input to the CX25800 can be used by an external audio or video processor to take advantage of the CX25800 on-board audio DACs.

The CX25800 supports multiple I²S formats for maximum flexibility when connecting to external devices. The bit width of the input samples can range from 16-32 bits, and the input sample rate can be 48, 96, 144, or 192 kHz. Sony or Philips-style formats are supported. If the input samples are larger than 16 bits, the LSBs beyond 16 bits are truncated. Because the data rate to the audio subsystem is 48 kHz, if incoming input samples are received at rates in excess of 48 kHz, the extra samples are dropped. For instance, if the input format is 24 bits at 96 kHz, the eight lowest LSBs are truncated, and every other sample are dropped.

The CX25800 can be configured as either an I²S master or a slave. As a master it generates the clock and word select. As a slave it receives the clock and word select from the external I²S source.

An autobaud feature determines the baud rate of the incoming I²S serial data stream. The detected baud can be read in the I²S Input Status register, bits 5:0.

24'h320120—I²SINPUT Register

Bits	Type	Default	Name	Description
[0]	RW	1'b0	NSlaveMaster	0 = CX25800 is slave 1 = CX25800 is master
[1]	RW	1'b0	NPhilipsSony	0 = Conform to Philips specification 1 = Conform to Sony specification
[2]	RW	1'b0	DisableAutoBaud	0 = Autobaud 1 = Disable autobaud
[15:3]	RO	13'h0000	—	Reserved

24'h320124—I²SINPUTSTATUS Register

Bits	Type	Default	Name	Description
[5:0]	RO	6'h000	Status	0 = 0 kHz 1 = 48 kHz 2 = 96 kHz 3 = 144 kHz 4 = 192 kHz 5 = 240 kHz (not supported) 6 = 288 kHz (not supported) > 6 => 288 kHz (not supported)
[15:6]	RO	9'h000	—	Reserved

2.1.6.2 I²S Output

The CX25800 supports I²S output to allow the user to bypass the built-in audio DACs and drive a Sony/Philips/Digital Interconnect Format (S/PDIF) driver for connection to a sound card, external surround processor, or digital recorder using an all-digital interface. In addition, this feature is useful when interfacing the CX25800 to a hardware MPEG II video and audio encoder for compression and synchronization between video and audio streams generated by the CX25800.

In I²S output mode, the CX25800 is always the master device. It generates the clock and word select.

Output muting is possible by asserting the Mute bit in the I²SOUTPUT register.

24'h320128—I²SOUTPUT Register

Bits	Type	Default	Name	Description
[0]	RW	1'b0	NPhilipsSony	0 = Conform to Philips specification 1 = Conform to Sony specification
[1]	RW	1'b0	Mute	Holds SCK, WS, and SD outputs
[15:2]	RW	14'h0000	—	Reserved

2.1.7 I²S Control

The CX25800 can be used in a wide variety of audio applications. To support as many I²S interface combinations as possible, the I²SCTL register provides several methods of multiplexing pins and signal information according to application. In addition to supporting timing master and slave modes on the I²S input interface, an over-sample clock output is provided for interfacing to external audio ADCs or DACs. The over-sample clock runs at 256 x the sample rate, which for 48 kHz audio is 12.288 MHz.

24'h3205EC- I²SCTL

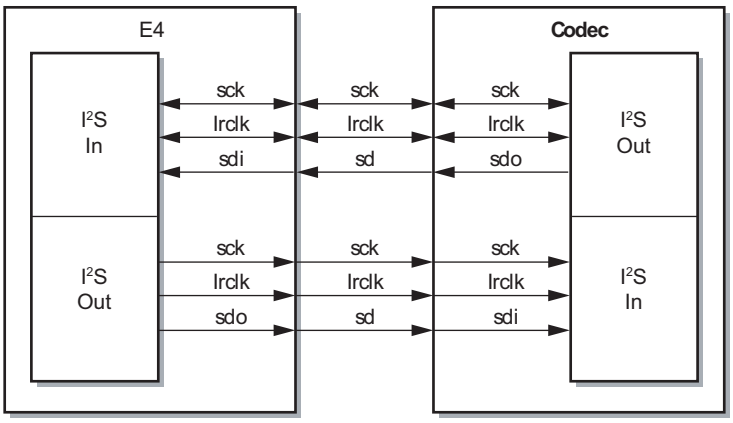
Bits	Type	Default	Name	Description
[0]	RW*	1'b0	OSCLK2SCKOUT	Send oversample clock out to the I²S Out sck (serial clock) pin
[1]	RW*	1'b0	OSCLK2SCKIN	Send oversample clock out to the I²S In sck (serial clock) pin. Forces output enables for I²S In pins to be high (output mode)
[2]	RW*	1'b0	I²SOUT2IN	Use I²S Out serial clock and word clock to drive I²S In block internally.
[3]	RW*	1'b0	I²SDIN2DOUT	Connects the I²S In serial data input directly to the I²S Out serial data output.
[15:4]	RW*	12'h0000		Reserved

The I²SCTL register supports five modes for audio interfacing to external audio ADCs, DACs and compression ICs.

2.1.7.1 Normal Mode

Normal mode operation supports transfer of audio samples to an MPEG Encoder/ CODEC or to a nyquist-rate audio ADCs and DACs. No oversample clock is provided, and each I^2S interface has its own dedicated three signals: SCK, LRCK, SDAT. This is illustrated in Normal Mode Operation. Normal mode is the default configuration. It can also be programmed by writing 0x0 to the I^2SCTL register.

Figure 4. Normal Mode Operation



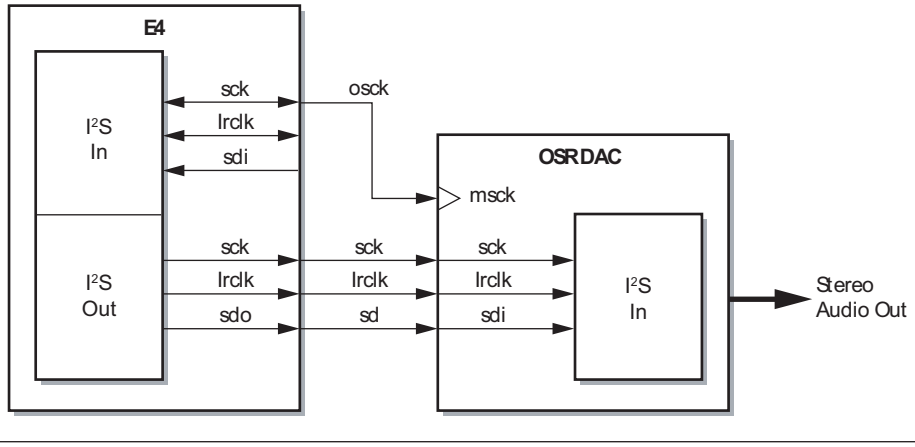
GENERAL NOTE:
1. I^2S In enabled.
2. I^2S Out enabled.
3. No oversample clock provided.

2.1.7.2 OSR DAC Mode

OSR DAC Mode is available to drive an external high quality stereo audio DAC which requires an oversampled clock. The I^2S input is not available in this mode. The I^2S input serial clock pin is used to output the oversampled clock. The I^2S output pins are still available.

OSR DAC mode is programmed by writing 0x2 to the I^2SCTL register. Additionally, the I^2SIN_ENABLE bit in the AUDCTL register must be disabled, and the I^2SOUT_ENABLE bit should be enabled. OSRDAC mode is illustrated in Figure 5.

Figure 5. OSR DAC Mode Operation



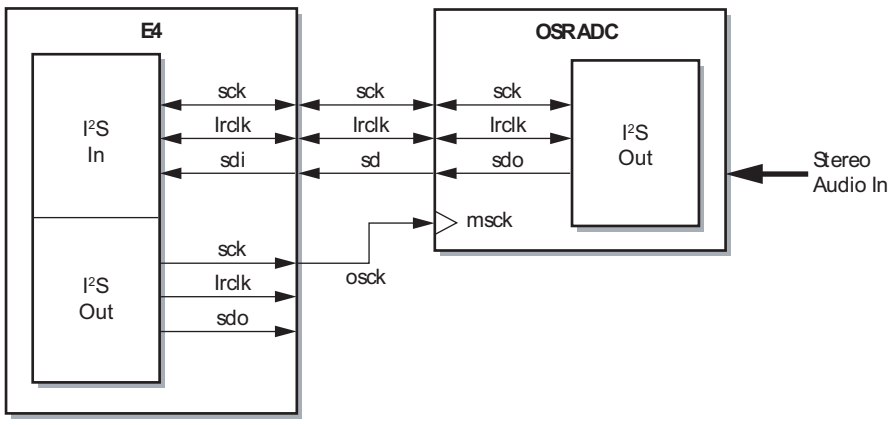
GENERAL NOTE:
1. I²S In disabled.
2. I²S Out enabled.
3. Oversample clock provided for DAC.

2.1.7.3 OSR ADC Mode

OSR ADC mode is available as an input for baseband stereo audio through an external audio ADC which requires an oversample clock. The I^2S output is not available in this mode. The I^2S output serial clock pin is used to output the oversampled clock. The I^2S input pins are still available for use.

OSR ADC mode is programmed by writing 0x1 to the I^2SCTL register. Additionally, the I^2SIN_ENABLE bit in the AUDCTL register should be enabled, and the I^2SOUT_ENABLE bit should be disabled. OSR ADC mode is illustrated in Figure 6.

Figure 6. OSR ADC Mode Operation



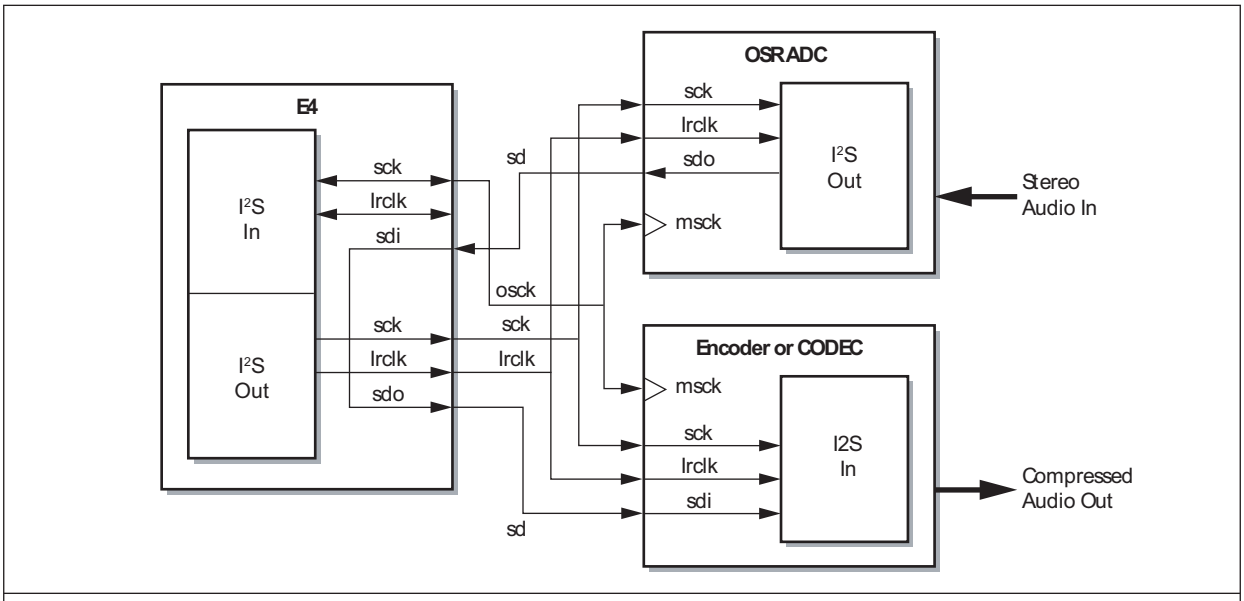
GENERAL NOTE:
1. I²S In enabled.
2. I²S Out disabled.
3. Oversample clock provided for ADC.

2.1.7.4 Passthrough Mode

Passthrough mode is provided as a method of making the CX25800 act as a multiplexer between its own digital output from the analog audio input and the digital output from an I²S input when either the I²S input or output (or both) require an oversample clock. In this mode, the oversample clock is sent to the I²S input serial clock pin. Both the external I²S devices are connected to the I²S output serial clock and word clock. The I²S input serial data pin is internally connected directly to the I²S output serial data output pin. Both of the external I²S devices must support slave-mode operation. This is illustrated in Figure 7.

Passthrough mode is programmed by writing 0x8 to the I²SCTL register. Additionally, the I²SIN_ENABLE bit in the AUDCTL register should be disabled, and the I²SOUT_ENABLE bit should be enabled.

Figure 7. Passthrough Mode Operation



GENERAL NOTE:

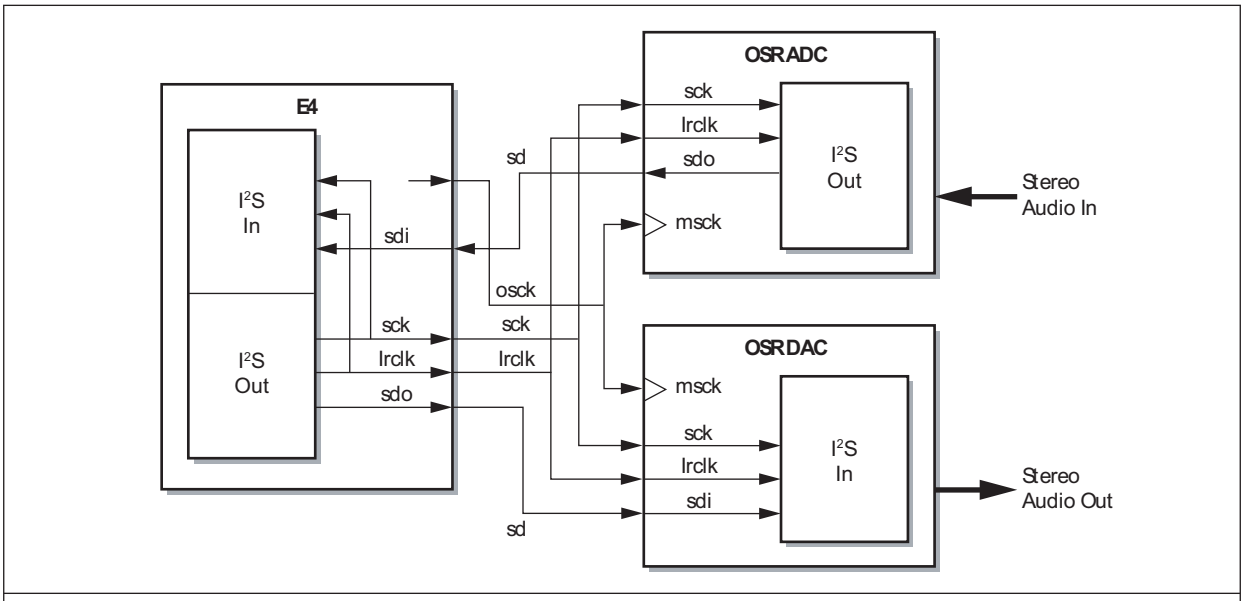
1. I²S In disabled.
2. I²S Out enabled.
3. External ADC and CODEC (or DAC) slaved to I²S Out.
4. I²S In serial data passed directly to I²S Out serial data.
5. Oversample clock provided for ADC and/or DAC.

2.1.7.5 Full Functionality Mode

Full functionality mode is available as a method for providing an oversampled clock to external I²S devices, while still maintaining separate I²S streams in and out. In this mode, the I²S input is internally slaved to the I²S output serial clock and word clock, the external devices are both connected to the I²S output serial clock and word clock, the oversample clock is provided on the I²S output serial clock pin, and only the serial data in to the I²S Input block and serial data out from the I²S Output block are kept separate. In this mode, it is possible to send data from the I²S output to a MPEG encoder or codec, while simultaneously streaming baseband audio in the I²S input over the PCI, enabling DVCR record-one, play-another functionality with composite source. Like the Passthrough mode, both I²S devices must support slave mode operation. This mode is illustrated in Figure 8.

Full functionality mode is enabled by programming 0x6 to the I²SCTL register, which enables the oversample clock output on the I²S input serial clock pin, and slaves the I²S input off the I²S output serial clock and word clock internally. Additionally, the I²SIN_ENABLE bit, and the I²SOUT_ENABLE bit in the AUDCTL register should be enabled. Finally, the NSLAVEMASTER bit in the I²SINPUT register should be disabled to put the I²S Input into slave mode.

Figure 8. Full Functionality Mode



GENERAL NOTE:

1. I²S In enabled.
2. I²S Out enabled.
3. External ADC and DAC slaved from I²S Out.
4. I²S In serial clock and word clock slaved from I²S Out.
5. Oversample clock provided for ADC and/or DAC.

2.1.8 Audio DACs

The CX25800 provides an analog stereo audio output that can drive a PC audio card or a stereo preamplifier input. Two integrated audio DACs provide approximately 85 dB SNR when used with an external active filter circuit, or approximately 75 dB SNR when used with a simple RC external construction filter. See Chapter 3 for external component example circuits.

The input to the audio DACs is based on two bits present in the AUD_CTL register: DAC_ENABLE and I^2S_STR2DAC. If DAC_ENABLE is disabled, then no signals or enables are passed to the DAC. If DAC_ENABLE is enabled, then either the I^2S input (if I^2S_STR2DAC is enabled) or the upstream DMA channel (if I^2S_STR2DAC is disabled) is passed to the DAC.

24'h32058C—AUD_CTL Register, Bits [12], [14]

Bits	Type	Default	Name	Description
[12]	RW	1'b0	DAC_ENABLE	DAC enable bit
[14]	RW	1'b0	I^2S_STR2DAC	I^2S input straight to DAC enable bit

The DAC output sample rate is a fixed divide off the PLL clock. The sample rate is calculated as the PLL frequency divided by 18 (the DAC pulse width modulated output rate) and divided by 128 (the DAC oversampling ratio). Whichever sample rate converter is used to drive the input to the DAC (through a FIFO) must be programmed to this sample rate, not the 48 kHz sample rate that is normally used. For instance, if the demodulator is used as the source to the DAC, the demodulator sample rate converter DDS frequency must be programmed to provide output samples at the calculated sample rate of the DAC instead of 48 kHz.

2.2 General Purpose Host Port

2.2.1 Introduction

The CX25800 features a general purpose bidirectional host processor interface. This enables board vendors to add additional components to a basic CX25800 design.

Table 2 gives some examples of peripherals that can be added.

Table 2. CX25800 Applications Enabled by Host Port Peripherals

Application	ICs that connect to the CX25800 General Purpose Host Port
Digital VCR	Conexant MPEG Encoder IC
Cable Modem PC/TV	Conexant Cable Modem IC
PC/TV with IR remote control	IR Controller
Video Editor	DV Codec

2.2.2 Host Port Overview

The GPHP supports peripherals that conform to either Motorola or Intel-style bus interface signaling protocols, with appropriate big endian vs. little endian byte ordering. The GPHP supports either discrete or multiplexed address/data buses as follows:

- 8-bit data path and 8-bit address on a nonmultiplexed bus
- 16-bit data path and 16-bit address on a multiplexed bus

The GPHP allows simultaneous connection to two peripheral ICs with no external interface logic, or four peripheral ICs with external glue logic. The function of the glue logic is to decode the chip select information encoded onto the two chip select pins when in encoded chip select mode. The GPHP can then be used to gain access to the memory map of these external devices for register reads and writes.

The GPHP interface is configurable through the host interface registers. These registers allow for the selection of the bus size, handshaking mode, signal polarity, and control signal timing adjustment.

The GPHP pin interface is defined in Table 19.

Table 3. GPHP Pin Definition

Pin Number	Pin Name	Dir	Full Name	Description: GPHP Signals
91, 92, 93, 94, 95, 96, 97, 98, 99, 100, 101, 106, 107, 108, 109, 110	HAD[15:0]	I/O	General Purpose Host Address/Data	Bidirectional address/data access bus. The width is selectable between an 8-bit address and 8-bit data bus, or a multiplexed 16-bit address/data bus.
90	HCS#	O	General Purpose Host Chip Select	External Chip select
89	HRD/HDS#	O	General Purpose Host Read/ Data Strobe	Either the active low read signal (Intel mode) or the programmable polarity data strobe signal (Motorola mode).
87	HWR/HRW#	O	General Purpose Host Write/ Read NOT Write	Either the active low write signal (Intel mode) or the read/ not write (Motorola mode).
88	HALE#	O	General Purpose Host Address Latch Enable	Address Latch Enable signal. Used only in multiplexed 16-bit address/data mode.
86	HRDY#	I	General Purpose Host Ready	External data transfer acknowledge signal
85	HEXFB	I	General Purpose Host External Status	Handshaking signal for use in DMA mode to indicate the status of the external source or destination FIFO.

Host Wait-State Control

24'h380054—HST_WSC Register

Bits	Type	Default	Name	Description
[31:28]	RW	4'h1	HST_W3W	Wait state control for external write cycles to chip select: HCS[3]#. Length of write cycle = (register value * bclk period).
[27:24]	RW	4'h1	HST_W2W	HCS[2] write cycle
[23:20]	RW	4'h1	HST_W1W	HCS[1] write cycle
[19:16]	RW	4'h1	HST_W0W	HCS[0] write cycle
[15:12]	RW	4'h1	HST_W3R	Wait state control for external read cycles to chip select: HCS[3]#. Length of write cycle = (register value * bclk period).
[11:8]	RW	4'h1	HST_W2R	HCS[2] read cycle
[7:4]	RW	4'h1	HST_W1R	HCS[1] read cycle
[3:0]	RW	4'h1	HST_W0R	HCS[0] read cycle

Host Transfer Control

24'h380058—HST_XFER_CNTL Register

Bits	Type	Default	Name	Description
[15]	RW	1'b0	Hcs3_cs_hold	HCS[3] chip select hold time (15 ns) relative to read or write enable (1 = On, 0 = Off)
[14]	RW	1'b0	Hcs2_cs_hold	HCS[2] chip select hold time
[13]	RW	1'b0	Hcs1_cs_hold	HCS[1] chip select hold time
[12]	RW	1'b0	Hcs0_cs_hold	HCS[0] chip select hold time
[11]	RW	1'b0	Hcs3_ds_polarity	External Data Strobe polarity for HCS[3](1 = positive, 0 = negative) Motorola mode only.
[10]	RW	1'b0	Hcs2_ds_polarity	External Data Strobe polarity for HCS[2]
[9]	RW	1'b0	Hcs1_ds_polarity	External Data Strobe polarity for HCS[1]
[8]	RW	1'b0	Hcs0_ds_polarity	External Data Strobe polarity for HCS[0]
[7]	RW	1'b0	Hcs3_xfer_mode	External Transfer mode for HCS[3](we# & re# or R/W# & ds#) (intel(0) or Motorola(1)
[6]	RW	1'b0	Hcs2_xfer_mode	External Transfer mode for HCS[2]
[5]	RW	1'b0	Hcs1_xfer_mode	External Transfer mode for HCS[1]
[4]	RW	1'b0	Hcs0_xfer_mode	External Transfer mode for HCS[0]
[3]	RW	1'b0	Hcs2_sh_extend	External data setup and hold time extend for HCS[3] (0 = 1x bclk period 1 = 2x bclk period)
[2]	RW	1'b0	Hcs2_sh_extend	External setup and hold extend for HCS[2]
[1]	RW	1'b0	Hcs1_sh_extend	External setup and hold extend for HCS[1]
[0]	RW	1'b0	Hcs0_sh_extend	External setup and hold extend for HCS[0]

Host Interface Width

24'h38005C—EXT_INTF_WIDTH Register

Bits	Type	Default	Name	Description
[3]	RW	1'b0	Ext_intf_width[3]	HCS3: (0): 16-bit (multiplexed), (1): 8-bit
[2]	RW	1'b0	Ext_intf_width[2]	HCS2: (0): 16-bit (multiplexed), (1): 8-bit
[1]	RW	1'b0	Ext_intf_width[1]	HCS1: (0): 16-bit (multiplexed), (1): 8-bit
[0]	RW	1'b0	Ext_intf_width[0]	HCS0: (0): 16-bit (multiplexed), (1): 8-bit

Host Peripheral Handshake

24'h380060—HRDY_HANDSHAKE Register

Bits	Type	Default	Name	Description
[3]	RW	1'b0	Mstr_handshake[3]	HCS3 HRDY handshake enable bit
[2]	RW	1'b0	Mstr_handshake[2]	HCS2 HRDY handshake enable bit
[1]	RW	1'b0	Mstr_handshake[1]	HCS1 HRDY handshake enable bit
[0]	RW	1'b0	Mstr_handshake[0]	HCS0 HRDY handshake enable bit

Host Multiplexed 16-bit Transfer Parameters

24'h380064—MUX16_PARAM Register

Bits	Type	Default	Name	Description
[31:28]	RW	4'b0001	HCS3_ale_timing	HCS3 HRDY handshake enable bit
[27:24]	RW	4'b0001	HCS2_ale_timing	HCS2 HRDY handshake enable bit
[23:20]	RW	4'b0001	HCS1_ale_timing	HCS1 HRDY handshake enable bit
[19:16]	RW	4'b0001	HCS0_ale_timing	HCS0 HRDY handshake enable bit
[15:12]	RW	4'b0010	HCS3_addr_cyc	HCS3 Address cycle width (register value * bclk period) setup time not included
[11:8]	RW	4'b0010	HCS2_addr_cyc	HCS2 Address cycle width
[7:4]	RW	4'b0010	HCS1_addr_cyc	HCS1 Address cycle width
[3:0]	RW	4'b0010	HCS0_addr_cyc	HCS0 Address cycle width

Host Chip Select Mode

24'h380068—HCS_MODE_SEL Register

Bits	Type	Default	Name	Description
[0]	RW	1'b0	HCS_mode_sel	This bit selects between the two possible chip select modes: 0: 2-bit dedicated chip selects. For times when two or fewer devices are connected to the host port. 1: 2-bit encoded chip selects. For times when more than two devices are connected to the host port.

Host Software Reset

24'h38C06C—HOST_SOFT_RST Register

Bits	Type	Default	Name	Description
[0]	WO	1'b0	HOST_SOFT_RST	Host Software Reset. Writing a 1 to this register triggers a reset of the host logic.

Host Interrupt Mask

24'h200090—HST_INT_MSK Register

Bits	Type	Default	Name	Description
[19:0]	RW	20'b0	HST_INT_MASK	A value of 1 enables the corresponding interrupt bit location in the HST_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

Host Interrupt Status

24'h200094—HST_INT_STAT Register

Bits	Type	Default	Name	Description
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[13]	RR	1'b0	UP_SYNC	Set when number of lines or bytes do not match the upstream host RISC program expectations.
[12]	RR	1'b0	DN_SYNC	Set when number of lines or bytes do not match the downstream host RISC program expectations.
[9]	RR	1'b0	UPF_UF	Set when upstream host FIFO underflow condition is being handled.
[8]	RR	1'b0	DNF_OF	Set when downstream host FIFO overflow condition is being handled.
[5]	RR	1'b0	UP_RISCI2	Set when the IRQ2 bit in a upstream host RISC instruction is set.
[4]	RR	1'b0	DN_RISCI2	Set when the IRQ2 bit in a downstream host RISC instruction is set.
[1]	RR	1'b0	UP_RISCI1	Set when the IRQ1 bit in a upstream host RISC instruction is set.
[0]	RR	1'b0	DN_RISCI1	Set when the IRQ1 bit in a downstream host RISC instruction is set.

Host Interrupt Masked Status

24'h200098—HST_INT_MSTAT Register

Bits	Type	Default	Name	Description
[19:0]	RO	20'b0	HST_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

Host Interrupt Set Status

24'h20009C—HST_INT_SSTAT Register

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	HST_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

The GPHP can support one upstream DMA (transfer from host to peripheral through the CX25800) and one downstream (transfer from peripheral to host through the CX25800) DMA channel active at any time. These DMA channels are configured by the EPHP DMA registers and are detailed in the following pages.

IPB DMAC Current Buffer Pointer

24'h3000A8—DMA31_PTR1 Register

24'h3000AC—DMA32_PTR1 Register

Bits	Type	Default	Name	Description
[23:2]	RO	22'hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Current Table Pointer

24'h3000E8—DMA31_PTR2 Register

24'h3000EC—DMA32_PTR2 Register

Bits	Type	Default	Name	Description
[23:2]	RW*	22'hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Buffer Limit

24'h300128—DMA31_CNT1 Register

24'h30012C—DMA32_CNT1 Register

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

24'h300168—DMA31_CNT2 Register

24'h30016C—DMA32_CNT2 Register

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.

General Purpose Counter (Immediate access)

24'h38C020—HSTD_GP_CNT Register

24'h38C024—HSTU_GP_CNT Register

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate access)

24'h38C030—HSTD_GP_CNT_CNTRL Register

24'h38C034—HSTU_GP_CNT_CNTRL Register

Bits	Type	Default	Name	Description
[1:0]	WO	2'b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

Host Interface Streaming Enable (Immediate Access)

24'h38C040—HST_STREAM_EN Register

Bits	Type	Default	Name	Description
[5]	RW	1'b0	HSTU_RISC_EN	RISC Controller enable for the host interface upstream DMA channel.
[4]	RW	1'b0	HSTD_RISC_EN	RISC Controller enable for the host interface downstream DMA channel
[1]	RW	1'b0	HSTU_FIFO_EN	Enable for pulling data out of the host upstream DMA FIFO or CDT.
[0]	RW	1'b0	HSTD_FIFO_EN	Enable for fetching downstream data from the external source.

Host Upstream DMA Control Register #1

24'h380048—HSTU_DMA_CTRL1 Register

Bits	Type	Default	Name	Description
[25]	RW	1'b0	UP_FIFO_HK_EN	Host upstream FIFO handshake enable. This enables the CX25800 to monitor the External_fifo_busy bit and act accordingly.
[24]	RW	1'b0	HSTU_AINC_EN	Host upstream address auto-increment enable. Used to DMA data to sequential addresses within the slave device. Not to be used when the destination is a FIFO.
[23:0]	RW	24'hxxxxxx	HSTU_DST_ADDR	HST upstream IPB DMA Destination address. If auto-increment is enabled then the value loaded into this register should be the starting address.

Host Downstream DMA Control Register #1

24'h38004C—HSTD_DMA_CTRL1 Register

Bits	Type	Default	Name	Description
[25]	RW	1'b0	DN_FIFO_HK_EN	Host downstream FIFO handshake enable. This enables CX25800 to monitor the External_fifo_busy bit and act accordingly.
[24]	RW	1'b0	HSTD_AINC_EN	Host downstream address auto-increment enable. Used to DMA data to sequential addresses within the slave device. Not to be used when the destination is a FIFO.
[23:0]	RW	24'hxxxxxx	HSTD_SRC_ADDR	HOST downstream IPB DMA source address. If auto increment is enabled then the value loaded into this register should be the starting address.

Host Downstream DMA Control Register #2

24'h380050—HSTD_DMA_CTRL2 Register

Bits	Type	Default	Name	Description
[11:0]	RW	12'b0	HST_LNGTH	HST downstream transfer count in bytes.

2.2.3 General Purpose Host Port Memory Space

The memory space associated with the GPHP is divided into two categories, internal registers and the external peripheral address space. Table 20 provides descriptions of each address range in the GPHP memory space.

Table 4. GPHP Memory Space

ADDRESS RANGE	SIZE	DESCRIPTION
380000–38FFFF	64 kB	HOST local registers, specific to the CX25800
390000–39FFFF	64 kB	Peripheral 1 address space
3A0000–3AFFFF	64 kB	Peripheral 2 address space
3B0000–3BFFFF	64 kB	Peripheral 3 address space
3C0000–3CFFFF	64 kB	Peripheral 4 address space

2.2.4 General Purpose Host Port Interface Register Access

There are 64 KB of address space available within the GPHP address space for each of the four possible peripherals and all of the registers pertaining to the GPHP configuration. For the peripherals that are connected to the CX25800 through the 8-bit data interface, only the lower 256 bytes of this space are accessible. This register mapping allows the peripherals to have their registers directly mapped into the CX25800 memory map.

2.2.5 General Purpose Host Interface External DMA Transfers

Streaming of data upstream and downstream is achieved through the DMA mechanism resident in the GPHP. There are two dedicated DMA channels that are available One channel is dedicated to upstream DMA while the other is dedicated to downstream DMA.

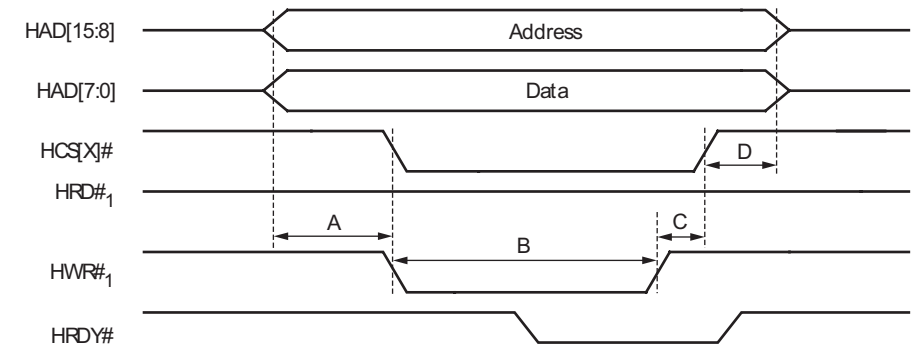
Once the DMAC is set up for the transfer, the GPHP must be configured. This configuration consists of the programming of the GPHP DMA Setup registers. For upstream transfers, the GPHP must be programmed with the external destination address, auto-increment enable/disable, and end-of-transfer interrupt enable. For downstream transfers, the GPHP must be programmed with the external source address, byte count, auto-increment enable/disable, and end-of-transfer interrupt enable. These reads and writes are then forwarded by the GPHP to the appropriate external source or destination address.

Upon completion of a packet of data, the GPHP generates the appropriate DMA interrupt.

The GPHP uses its external FIFO status pin to interface with an external streaming FIFO. When enabled, this pin is used to indicate when the external destination can safely accept more data in the upstream case, and when the external source has data to transfer in the downstream case. Because there are two DMA channels and only one FIFO status pin, one of the two DMA channels must use the register polling approach to obtain the FIFO status in the case where both channels are being used simultaneously.

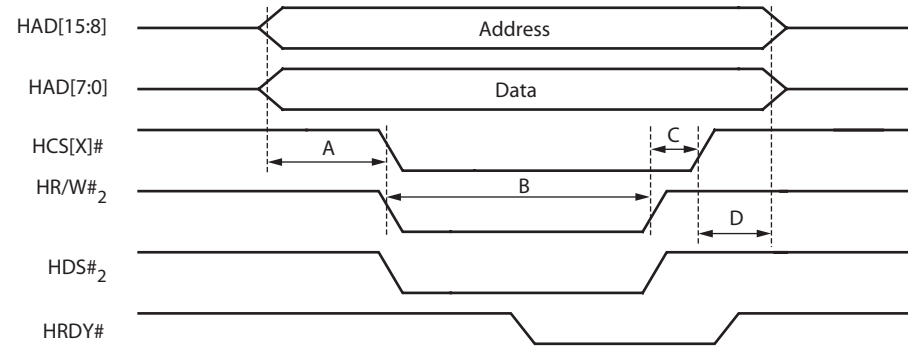
2.2.6 General Purpose Host Interface Signaling—Nonmultiplexed Mode

Figure 9. Host Interface Write Operation—Intel Style (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# has programmable polarity. HRDY# is shown here in its default setting, active low.

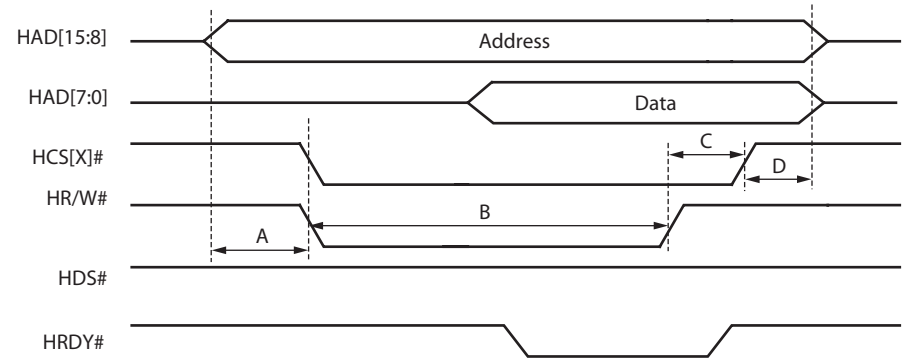
Figure 10. Host Interface Write Operation—Motorola Style (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# and HDS# each have programmable polarity. Both are shown here in their default settings, active low.

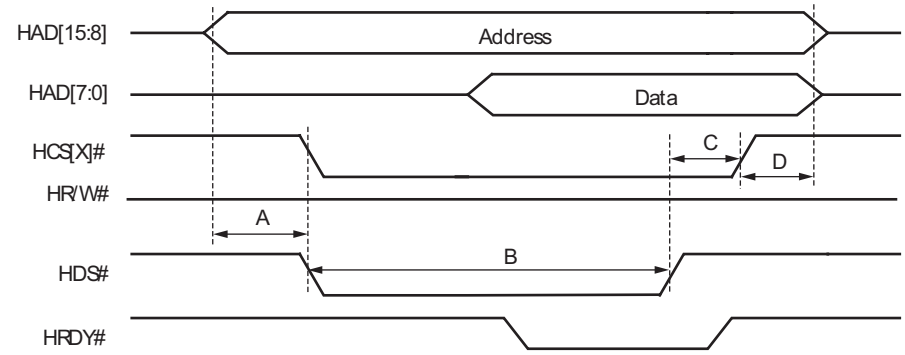
Description		Min	Max
A	Addr/Data setup time relative to write pulse and chip select and HDS pulse	1x PCLK Period	2x PCLK Period
B	Write pulse width, HDS pulse width	1x PCLK Period	15x PCLK Period
C	Chip select hold time relative to write pulse and HDS pulse	0	1x PCLK Period
D	Addr/Data hold time relative to chip select	1x PCLK Period	2x PCLK Period

Figure 11. Host Interface Read Operation—Intel Style (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# has programmable polarity. HRDY# is shown here in its default setting, active low.

Figure 12. Host Interface Read Operation—Motorola Style (Accessing an External Device)

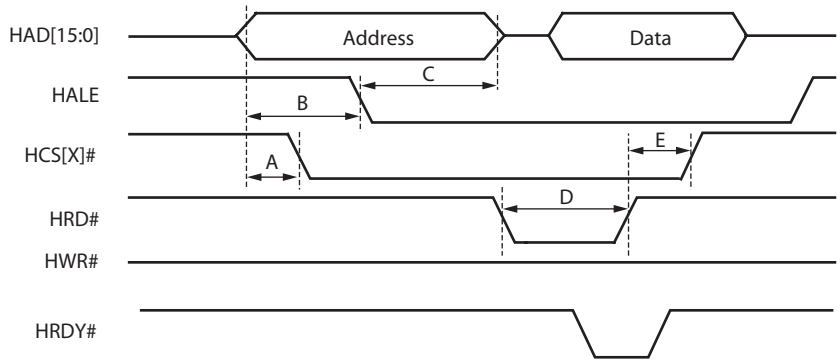


GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# and HDS# each have programmable polarity. Both are shown here in their default settings, active low.

Description		Min	Max
A	Addr/Data setup time relative to write pulse and chip select and HDS pulse	1x PCLK Period	2x PCLK Period
B	Write pulse width, HDS pulse width	1x PCLK Period	15x PCLK Period
C	Chip select hold time relative to write pulse and HDS pulse	0	1x PCLK Period
D	Addr hold time relative to chip select	1x PCLK Period	2x PCLK Period

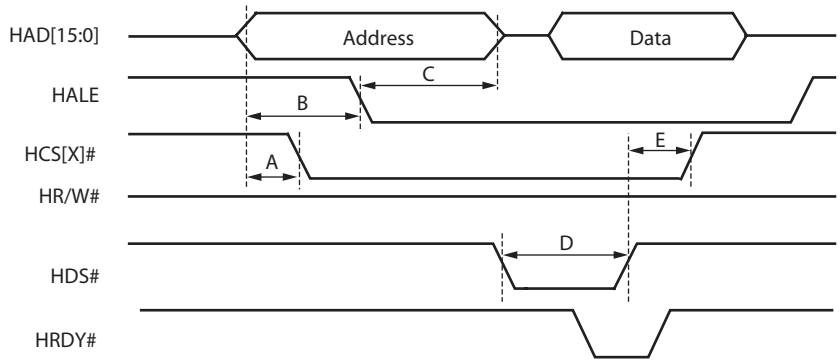
2.2.7 General Purpose Host Interface Signaling—Multiplexed Mode

Figure 13. Host Interface Read Operation—Intel Style Multiplexed Address/Data Bus (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# has programmable polarity. HRDY# is shown here in its default setting, active low.

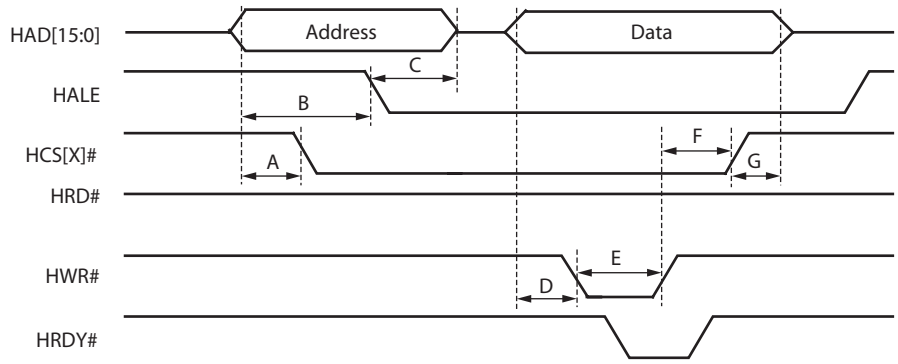
Figure 14. Host Interface Read Operation—Motorola Style Multiplexed Address/Data Bus (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# and HDS# each have programmable polarity. Both are shown here in their default settings, active low.

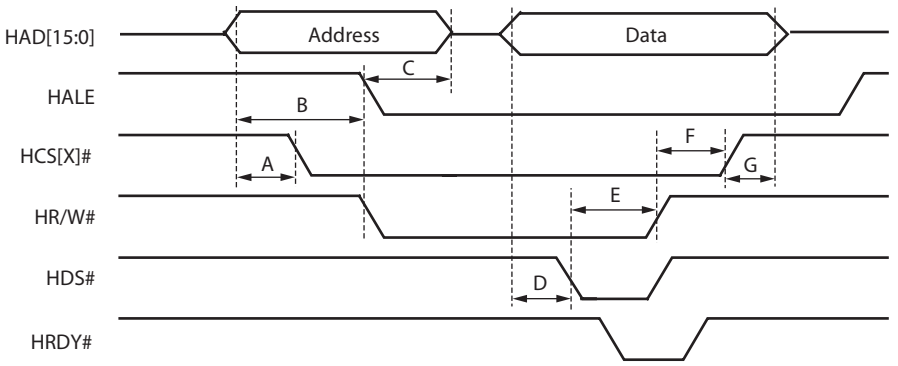
Description		Min	Max
A	Addr/Data setup time to chip select	1x PCLK Period	2x PCLK Period
B	Addr setup time relative to HALE	2x PCLK Period	3x PCLK Period
C	Chip select hold time relative to address latch enable	1x PCLK Period	1x PCLK Period
D	Read pulse width, HDS pulse width	1x PCLK Period	15x PCLK Period
E	Chip select hold time relative to read pulse and HDS pulse	0	1x PCLK Period

Figure 15. Host Interface Write Operation—Intel Style Multiplexed Address/Data Bus (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# has programmable polarity. HRDY# is shown here in its default setting, active low.

Figure 16. Host Interface Write Operation—Motorola Style Multiplexed Address/Data Bus (Accessing an External Device)



GENERAL NOTES:
1. The HRDY# signal only used for handshaking when it is enabled via one of the host registers.
2. HRDY# and HDS# each have programmable polarity. Both are shown here in their default settings, active low.

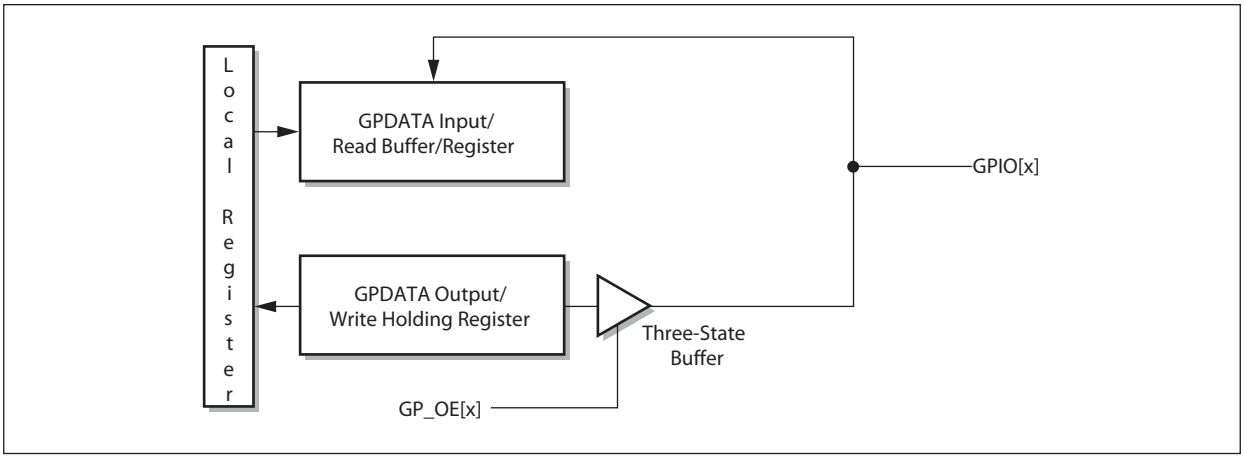
	Description	Min	Max
A	Addr setup time relative to chip select	1x PCLK Period	2x PCLK Period
B	Addr setup time relative to address latch enable (hale) and HR/W#	2x PCLK Period	3x PCLK Period
C	Addr hold time relative to address latch enable (hale)	1x PCLK Period	1x PCLK Period
D	Data setup relative to (Intel) write pulse or (Moto) HDS pulse	1x PCLK Period	1x PCLK Period
E	(Intel) Write pulse width (Moto) HDS pulse width	1x PCLK Period	15x PCLK Period
F	Chip select hold time relative to write pulse and HDS pulse	0	1x PCLK Period
G	Data hold time relative to the chip select	1x PCLK Period	2x PCLK Period

2.3 GPIO

2.3.1 GPIO Pin Architecture

Each GPIO pin is set up as a basic I/O buffer, with each bit of the General Purpose Output Enable (GPOE) register used to enable an individual pin's output driver (see Figure 17).

Figure 17. GPIO Pin Architecture



2.3.2 GPIO Modes in CX25800

Twenty-four pins are provided for GPIO. They are mapped onto the pin numbers listed in Table 21.

Table 5. GPIO Pin Numbers

Pin Numbers	GPIO Number
8–15	[23–16]
112–119	[15–8]
123–130	[7–0]

The GPIO port is highly flexible and can be assigned to the following functions with the CX25800. See Table 1.

- GPIO functions
- MPEG input parallel port (DVB common interface-compatible)
- VIP parallel host port expansion
- Digital video output from the video decoder as either 8-bit or 10-bit, 4:2:2 samples with 601-like external synchronization signals
- Digital video output from the video decoder as 8-bit, *ITU-R656*, 27 MHz, 4:2:2 samples
- Digital video input to the CX25800 image scaler (and subsequent DMA to VGA overlay surface) from an external MPEG decoder outputting *ITU-R656*, 27 MHz, 4:2:2 interlaced samples or 54 MHz, noninterlaced video samples
- General purpose host port external chip select function

The PINMUX_IO register is used to configure the entire GPIO port as desired. On power-up or PCI reset, all GPIO pins are undedicated. The 8 bits of the PINMUX_IO register [7:0] can be used to select any of 9 different basic functional usage configurations. Combinations of modes are possible, provided I/O pins do not overlap. The priority with respect to pin allocation to a desired function is from bit 7 down to bit 0. Therefore, if multiple GPIO modes are selected, the modes with the higher index are dominant and overwrite the functional meaning of pins selected by the lower index modes. In other words, MPEG_PAR_EN takes priority over VIP_MODE.

24'35C044—PINMUX_IO

Bits	Mode	Default	Program	Mode Name	Description
[7]	1	0	1	MPEG_PAR_EN	MPEG parallel port
[6:5]	2/3	00	xx	VIP_MODE	VIP host port width
[4]	4	0	1	VID_SYNC_EN	601 Video external output syncs
[3]	5	0	1	VID8_OUT_EN	656 Video 8-bit output port
[2]	6	0	1	VID10_OUT_EN	656 Video 10-bit output port
[1]	7	0	1	VID_IN_EN	656 Video input port
[0]	8	0	1	HCS1_EN	Host port chip select

Table 6 illustrates which modes can be used with other modes and which are mutually exclusive. Table 7 illustrates the GPIO mode versus pin usage.

NOTE: MPEG_PAR_EN, VIP4_MODE, VIP8_MODE, and HCS1_EN are extensions of the existing serial MPEG port, 2-bit VIP Host Master port, and GPHP, which are available at all times, irrespective of GPIO configuration.

Table 6. GPIO Mode Allocation

Mode Name	GPIO Pins																						
	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23
MPEG_PAR_EN																	X	X	X	X	X	X	X
VIP4_MODE																	X	X						
VIP8_MODE																	X	X	X	X	X	X		
VID_SYNC_EN	X	X	X	X	X	X	X																	
VID8_OUT_EN									X	X	X	X	X	X	X	X								
VID10_OUT_EN									X	X	X	X	X	X	X	X							X	X
VID_IN_EN	X	X	X	X	X	X	X	X																
HCS1_EN																								X

GENERAL NOTES:
1. X = Used in that mode; blank is unused and the pin is available for normal GPIO.

Table 7. GPIO Mode versus Pin Usage (1 of 2)

Default Power-Up Reset State		PINMUX_IO		PINMUX_IO		PINMUX_IO		PINMUX_IO	
Pin	Dir	MPEG_PAR_EN=1		VIP_MODE=01		VIP_MODE=10		HCS1_EN=1	
		Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir
GPIO[23]	I/O	Tsdat[1]	I					HCS[1]#	O
GPIO[22]	I/O	Tsdat[2]	I						
GPIO[21]	I/O	Tsdat[3]	I			VHAD[7]	I/O		
GPIO[20]	I/O	Tsdat[4]	I			VHAD[6]	I/O		
GPIO[19]	I/O	Tsdat[5]	I			VHAD[5]	I/O		
GPIO[18]	I/O	Tsdat[6]	I			VHAD[4]	I/O		
GPIO[17]	I/O	Tsdat[7]	I	VHAD[3]	I/O	VHAD[3]	I/O		
GPIO[16]	I/O			VHAD[2]	I/O	VHAD[2]	I/O		

Table 7. GPIO Mode versus Pin Usage (2 of 2)

Default Power-Up Reset State		PINMUX_IO		PINMUX_IO		PINMUX_IO		PINMUX_IO	
Pin	Dir	MPEG_PAR_EN=1		VIP_MODE=01		VIP_MODE=10		HCS1_EN=1	
		Signal	Dir	Signal	Dir	Signal	Dir	Signal	Dir
GPIO[23]	I/O					VDO[1]	O		
GPIO[22]	I/O					VDO[0]	O		
GPIO[21]	I/O								
GPIO[20]	I/O								
GPIO[19]	I/O								
GPIO[18]	I/O								
GPIO[17]	I/O								
GPIO[16]	I/O								
GPIO[15]	I/O			VDO[9]	O	VDO[9]	O		
GPIO[14]	I/O			VDO[8]	O	VDO[8]	O		
GPIO[13]	I/O			VDO[7]	O	VDO[7]	O		
GPIO[12]	I/O			VDO[6]	O	VDO[6]	O		
GPIO[11]	I/O			VDO[5]	O	VDO[5]	O		
GPIO[10]	I/O			VDO[4]	O	VDO[4]	O		
GPIO[9]	I/O			VDO[3]	O	VDO[3]	O		
GPIO[8]	I/O			VDO[2]	O	VDO[2]	O		
GPIO[7]	I/O							VDI[7]	I
GPIO[6]	I/O	V_NVRESET	O					VDI[6]	I
GPIO[5]	I/O	V_NHRESET	O					VDI[5]	I
GPIO[4]	I/O	V_HACTIVE	O					VDI[4]	I
GPIO[3]	I/O	V_VACTIVE	O					VDI[3]	I
GPIO[2]	I/O	V_CBFLAG	O					VDI[2]	I
GPIO[1]	I/O	V_FIELD	O					VDI[1]	I
GPIO[0]	I/O	V_VALID	O					VDI[0]	I

2.3.3 GPIO Normal Mode

The GPIO Port Normal mode can be used to input or output general board-level signals to or from the CX25800. The PINMUX_IO bits are in the default state of 32'h0000 during Normal mode. When in Normal mode, these pins are not designed to support a high speed interface for video or broadband data. For such applications, the other modes must be used.

24'h350010—GP0_IO Register

24'h350014—GP1_IO Register

24'h350018—GP2_IO Register

24'h35001C—GP3_IO Register

Bits	Type	Default	Name	Description
[31:26]	RO	6'h00		Reserved
[25]	RW	1'b0	GP3_MODE	A value of 0 enables the GPIO register interface in default mode where each set of 8 pins are controlled by a GP{x}_IO register. A value of 1 enables all 24 GPIO and/or GPOE bits to be read/ written simultaneously.
[24]	RO	1'b0		Reserved
[23:16]	Wd		GP{x}_BWE	If this field is equal to 8'h00, then the whole GPIO byte register operates in normal R/W mode. If any bit is set, then the corresponding GP_OE and GP_IO bit locations are enabled for writing. If the bit write enable is not set, the corresponding GPIO bits are unaffected.
[15:8]	RW	8'h00	GP{x}_OE	A value of 1 enables corresponding GP_IO bit to be output on the GPIO pin.
[7:0]	RW*	8'h00	GP{x}_IO	Writing provides data for GPIO output pin drivers. Reading accesses data directly from input pin buffers.

Note that the GP3_* control bits are only available in register GP3_IO. If GP3_MODE is set to 24-bit access mode, the GPIO register interface loses bit resolution field control capability.

24'h350010—GPIO

Bits	Type	Default	Name	Description
[23:0]	RW*	24'h000000	GP_IO	Writing provides data for GPIO output pin drivers. Reading accesses data directly from input pin buffers.

24'h350014—GPOE

Bits	Type	Default	Name	Description
[23:0]	RW*	24'h000000	GP_OE	A value of 1 enables corresponding GP_IO bit to be output on the GPIO pin.

In addition to capturing or generating simple input/output signals, some GPIO pins can service externally generated interrupts. GPIO [23:22] (pins 8 and 9) have input interrupt capability. The GPIO_ISM register allows control of input signal polarity and level or edge sensitivity.

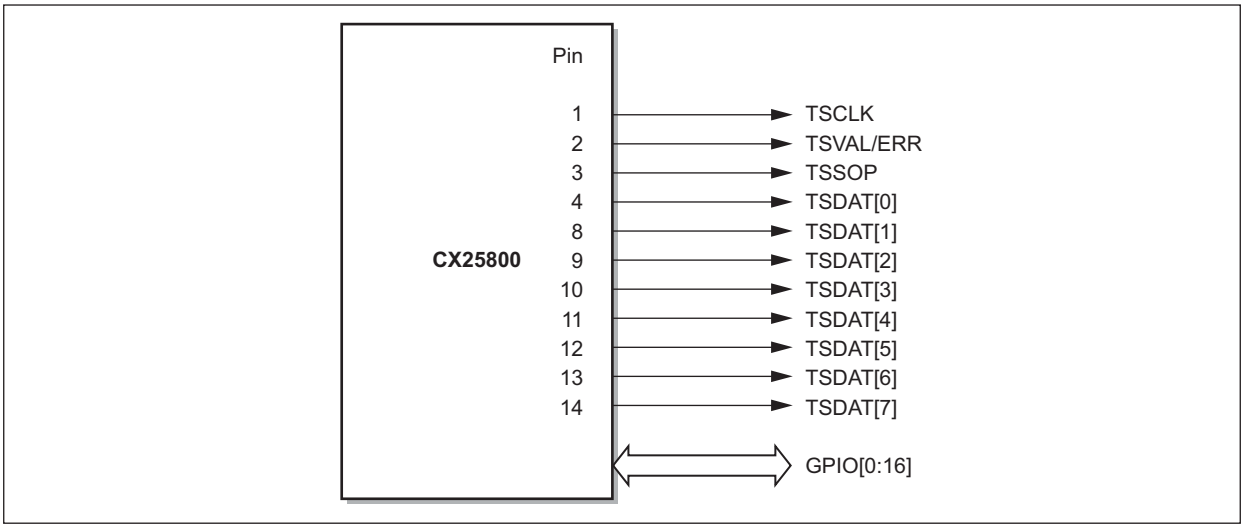
24'h350028—GPIO_ISM

Bits	Type	Default	Name	Description
[3:2]	WO	2'b00	GP_ISM_SNS	Sensitivity mode for interrupt inputs GPIO[23:22]. 0 = level-sensitive 1 = edge-sensitive
[1:0]	WO	2'b00	GP_ISM_POL	Polarity control for interrupt inputs GPIO[23:22]. 1 = active-hi or posedge 0 = active-lo or negedge

2.3.4 MPEG Parallel Port

Table 7 indicates that setting the PINMUX_IO register to 8'h80 enables the MPEG_PAR_EN mode. This means that the existing serial MPEG port is augmented by GPIO [17:23] to enable a full parallel MPEG input port for connection of DVB channel demodulators (which typically use an 8-bit data interface conforming to ETSI document EN 50221). Alternatively, MPEG encoders outputting compressed data over an 8-bit path should use this mode. GPIO [0:16] become available for other functions such as 4:2:2 video input, output, or GPIO. This is illustrated in Figure 18.

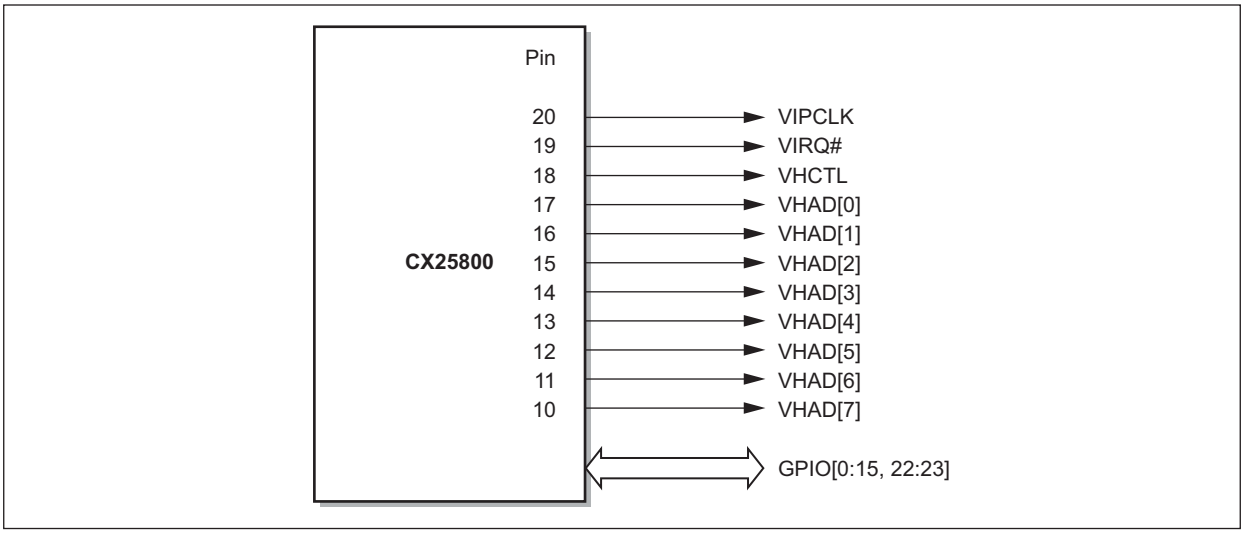
Figure 18. MPEG Parallel Port



2.3.5 8-Bit Parallel VIP Host Master

Table 7 indicates that setting the PINMUX_IO register to 8'h40 enables the 8-bit VIP Host Port mode. This means that the existing 2-bit VIP Host Port mode is augmented by GPIO [16:21] to enable a full 8-bit parallel VIP Host Master interface for connection of high performance digital video or graphics peripherals. GPIO [0:15,22:23] become available for other functions such as 4:2:2 video input, output, or GPIO. As seen from Table 7, this mode is mutually exclusive from MPEG_PAR_EN. This mode is not available on the CX25800. See Figure 19.

Figure 19. 8-bit Parallel VIP Host Master



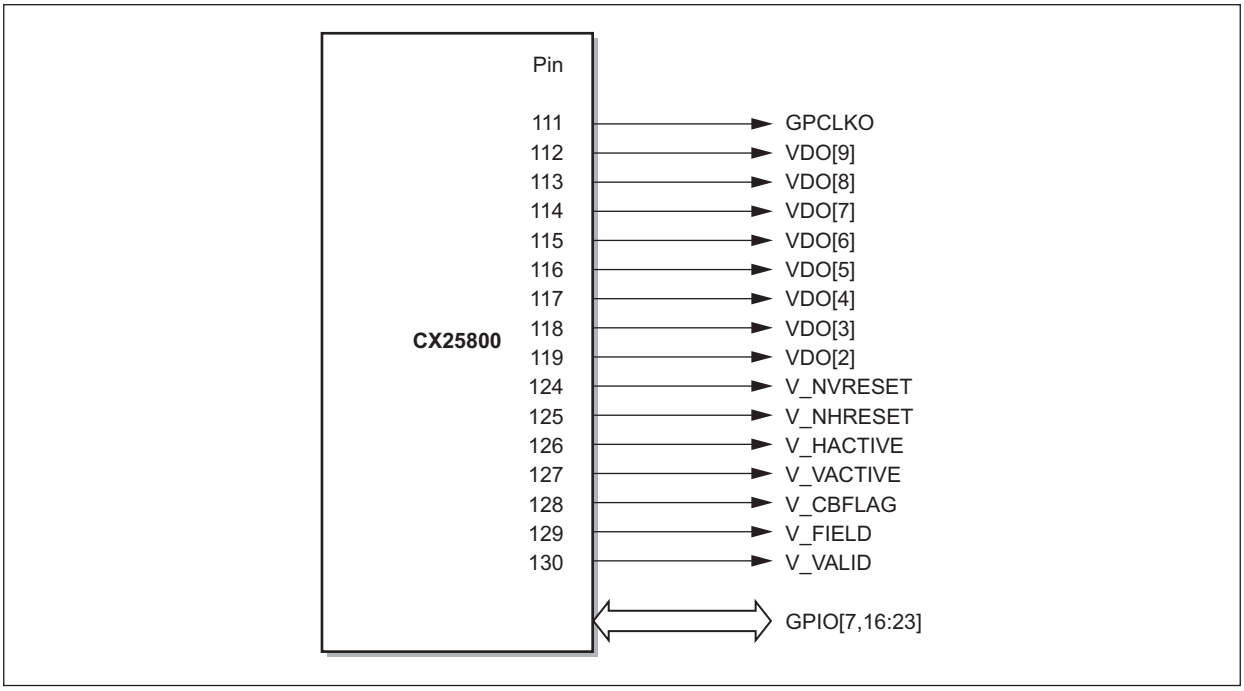
2.3.6 4-Bit Parallel VIP Host Master

Table 7 indicates that setting PINMUX_IO register to 8'h20 enables the 4-bit VIP Host Port mode. This means that the existing 2-bit VIP Host Port mode is augmented by GPIO [16:17] to enable a 4-bit parallel VIP Host Master interface for connection of medium performance digital video or graphics peripherals. GPIO [0:15, 18:23] become available for other functions such as 4:2:2 video input, output, or GPIO. As seen from Table 7, this mode is mutually exclusive from MPEG_PAR_EN.

2.3.7 Video Synchronous Pixel (SPI) Mode

This mode enables 8- or 10-bit 4:2:2 data to be output from the CX25800 to an external compressor or hardware deinterlacing integrated circuit, etc., which may not implement embedded video synchronization codes as used in ITU-R. *BT656* or *VIP 1.1* standards. If discrete video synchronization signals are required, this mode, invoked by setting PINMUX_IO register to 8'h08, should be used. As seen in Table 7, the GPIO [0:6] pins provide external synchronization signals, GPIO [8:15] pins are used for 8-bit 4:2:2 output samples, and GPIO [7, 16:23] pins are available for other functions. See Figure 20.

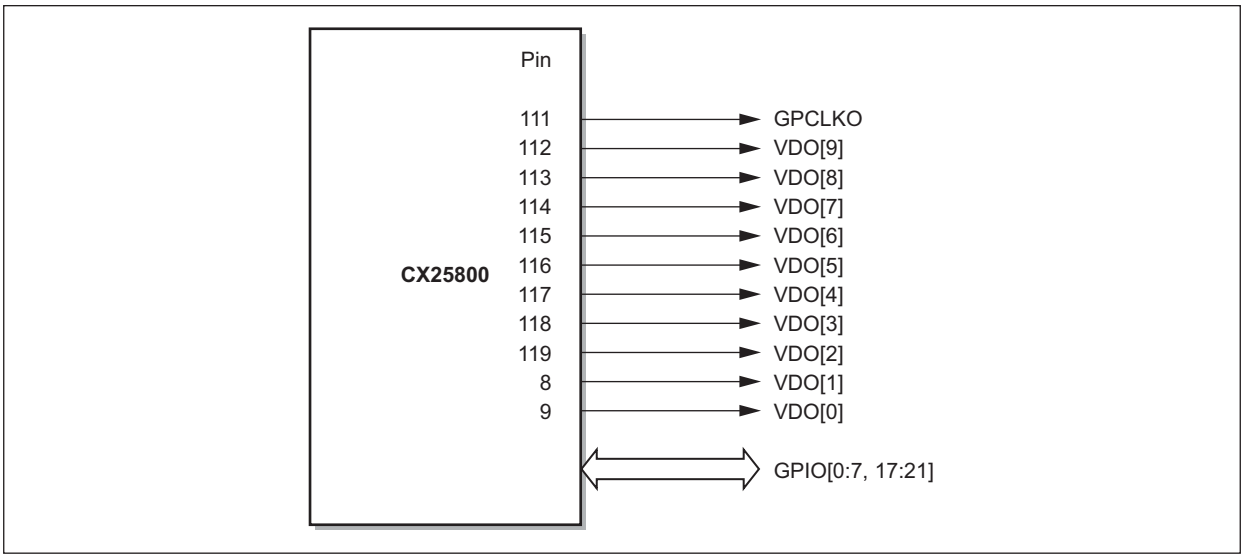
Figure 20. Video Synchronous Pixel (SPI) Mode



2.3.8 10-Bit ITU-R. BT656 Output Mode

This mode enables 10-bit 4:2:2 data to be output from the CX25800 to an external compressor or hardware deinterlacing integrated circuit etc. which implements embedded video synchronization codes as used in ITU-R. BT656 or VIP 1.1 standards. This mode is invoked by setting PINMUX_IO register to 8'h04. Table 7 indicates that the GPIO [8:15, 22:23] pins are used for 10-bit 4:2:2 output samples, and the GPIO [0:7, 16:21] pins are available for other functions. See Figure 21.

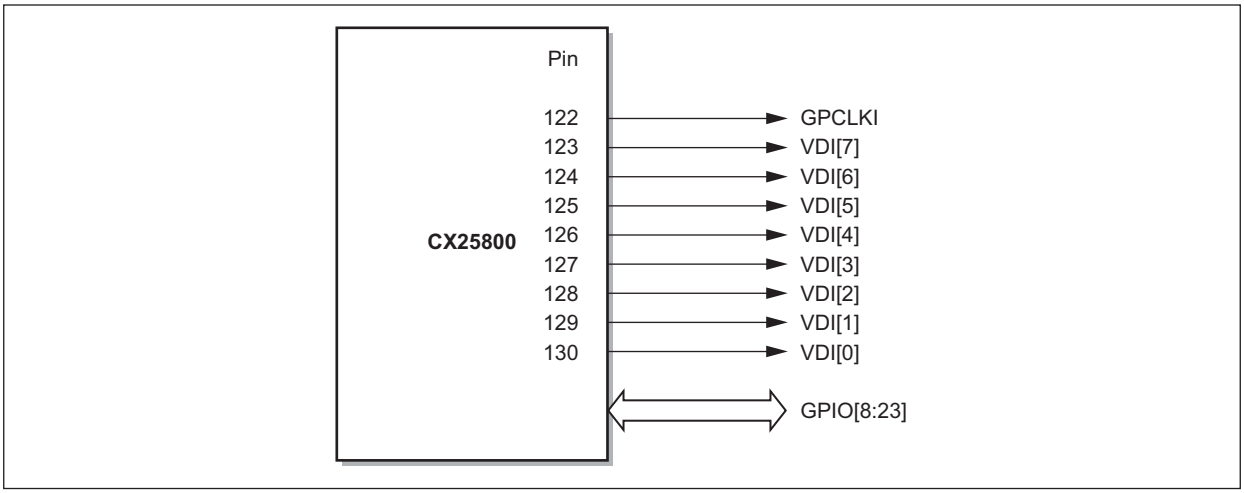
Figure 21. 10-bit ITU-R. BT656 Output Mode



2.3.9 8-Bit ITU-R. BT656/VIP 2.0 Pixel Input Mode

This mode enables 8-bit 4:2:2 data to be input to the CX25800 from an external video de-compressor for scaling and DMA transfer to a VGA overlay surface for display. The incoming video data must adhere to 27 MHz ITU-R. BT656/VIP 1.1 or 8-bit VIP 2.0 pixel data at a maximum data rate of 54 MHz. This mode is configured by setting PINMUX_IO register to 8'h02. Table 7 indicates that the GPIO [0:7] pins are used for 8-bit 4:2:2 input samples, and the GPIO [8:23] pins are available for other functions. See Figure 22.

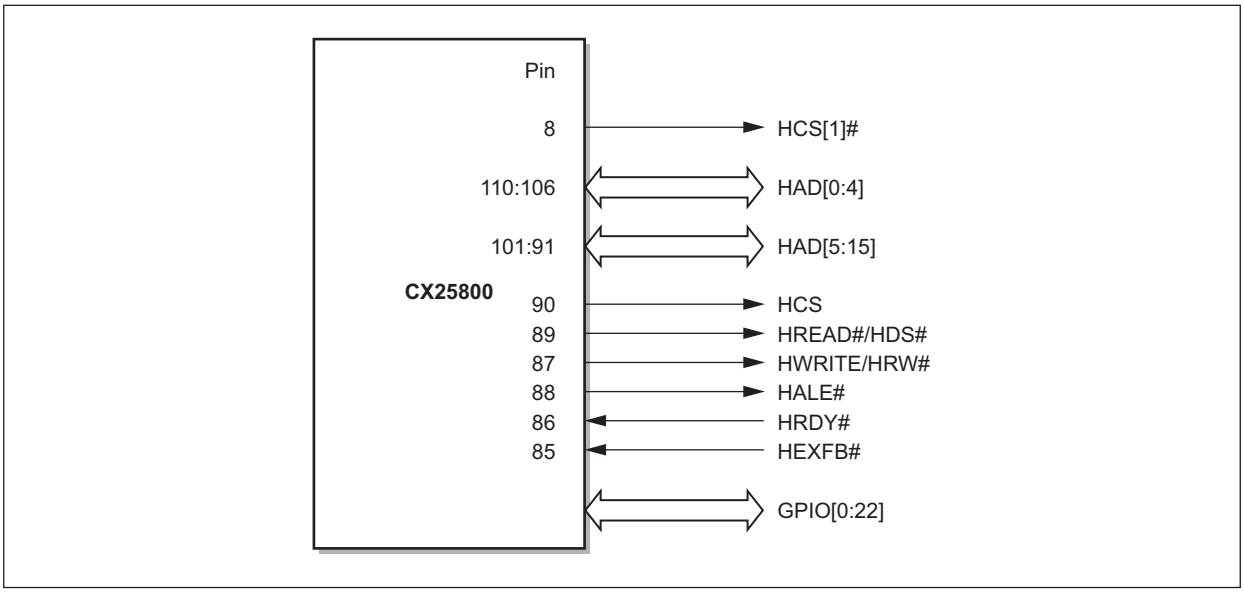
Figure 22. 8-bit ITU-R. BT656/VIP 2.0 Pixel Input Mode



2.3.10 Host Port Chip Select Enable Mode

This mode enables four external peripheral devices to be connected to the CX25800 GPHP with simple glue decode logic. In conjunction with Pin 90 (HCS), GPIO[23] becomes a second chip select pin, thus enabling selection of up to four external peripherals. This mode is configured by setting PINMUX_IO register to 8'h01. Table 7 indicates that GPIO [23] is used as the HCS[1] pin and the GPIO[0:22) pins are available for other functions. See Figure 23.

Figure 23. Host Port Chip Select Enable Mode



2.4 Peripheral Component Interface

The Peripheral Component Interface (PCI) subsystem contains the interfaces, data buffers, and control registers to allow the high integrity, high bandwidth transfer of data between the CX25800 and the host. The subsystem is very flexible to allow being tailored to fit the many possible applications. Many features have been incorporated to enable the handling of PCI bus latencies with minimal data loss. Data is buffered internally using a programmable SRAM based architecture, and transferred using a unique RISC and DMA controller architecture. The PCI subsystem also allows the host to access all internal memory, internal registers and external peripheral registers. The interface is implemented as a 32-bit wide, 33-MHz data path that conforms to the *PCI Local Bus Specification revision 2.3*.

2.4.1 PCI Functions

The five peripherals of the CX25800 are assigned to the PCI functions detailed in Table 8.

Table 8. PCI Functions

Function	Peripheral
0	Video
1	Audio
2	Transport Stream
3	VIP Host Port
4	GPHP

The CX25800 is configurable to have from one to five PCI functions depending on a particular application. For example, if an application only uses video, audio, and transport stream, the VIP Host Port and GPHP functions can be disabled. This is useful to eliminate the need for software drivers for unnecessary functions. Any combination of functions can be enabled or disabled, with the exception that function 0 cannot be disabled as required by the PCI specification.

Functions one through five are enabled using bits [1:4] of two-wire serial interface address 15'h5000, respectively, in the two-wire serial interface EEPROM which are automatically loaded into the CX25800 at reset. While the functions are automatically being configured after reset, any PCI accesses to the CX25800 are retried, to ensure that the PCI configuration space is established before the PCI system BIOS begins to access it. If no two-wire serial interface EEPROM is connected to the CX25800 through the two-wire serial interface, all functions are disabled except for function 0. The EEPROM can be programmed before being placed on the printed circuit board (PCB), or it can be written using the CX25800 two-wire serial interface control registers or the Vital Product Data (VPD) mechanism.

2.4.2 PCI Configuration Space

Each enabled function has its own PCI configuration space. To allow independent control, there are separate registers for each of the following functions:

- Device ID
- Command
- Status
- Master Latency Timer
- Maximum Latency
- Minimum Grant
- Interrupt Line
- Base Address
- Power Management

A few registers, which contain information common to all functions, are shared although they appear in the configuration spaces of all functions (e.g., Vendor ID, Subsystem Vendor, Subsystem ID, and Vital Product Data). The CX25800 does not respond to an attempted configuration space access to a disabled function, and therefore the access terminates with a Master Abort, as required by the PCI specification.

2.4.3 PCI Subsystem IDs

The Subsystem ID and Subsystem Vendor ID registers are automatically loaded at reset with the data located in the two-wire serial interface EEPROM at two-wire serial interface address 15’h5004 through 15’h5007. While the registers are being loaded after reset, any PCI accesses to the CX25800 are retried, to ensure that the Subsystem ID and Subsystem Vendor ID are established before the PCI system BIOS begins to access them. If no two-wire serial interface EEPROM is connected to the CX25800 through the two-wire serial interface, the Subsystem ID and Subsystem Vendor ID registers are loaded with 0. The EEPROM can be programmed before being placed on the printed circuit board (PCB), or it can be written using the CX25800 two-wire serial interface control registers or the Vital Product Data (VPD) mechanism. The Subsystem ID and Subsystem Vendor ID registers can also be written directly by software. To enable this, the SVIDS_EN bit in the Device Control #1 register must be first written to a 1.

2.4.4 Accessing VPD on the CX25800

To access the I²C EEPROM on the CX25800, the software application must add 15'h5008 to the address.

A typical example is when the application program needs to access memory address 15'h0020 in the I²C EEPROM. The application program must add 15'h5008 to the 15'h0020 address. The sum 15'h5028 is then written in the VPD_ADRS register.

The application program must add 15'h5008 to the address because there is no re-mapping of the I²C EEPROM in the CX25800. VPD starts at the physical address of 16'h5008. The 15-bit physical address maps directly to the EEPROM physical storage space. Addresses 11'h000-11'h007 are reserved in the EEPROM for function enables and Subsystem Vendor ID. Therefore, the first available VPD address is 15'h5008.

The two-wire serial interface EEPROM can be read any time by using the two-wire serial interface hardware, software, or direct mode.

2.4.5 PCI Specification Regarding VPD Implementation

Section 6.4 (Vital Product Data) in PCI Specification revision 2.3 states that implementation of VPD is optional. In addition, operating systems such as Microsoft Windows and system BIOS do not access VPD data during the PCI configuration cycle of the system.

2.4.6 Using VPD Data with Multiple Functions on One Card

Function 0 for video is the only function that uses VPD. This is permitted as indicated by the fourth paragraph preceding Figure I-2 in Appendix-I of *PCI Specification revision 2.3.*

2.4.7 PCI Power Management

The CX25800 implements the power management mechanism according to the PCI Bus Power Management Interface Specification Revision 1.1. Power states D0 (on), D3cold (off), and D3hot are supported. When the power state of all enabled functions is D3hot, the CX25800 goes into a low-power consumption mode.

2.4.8 Memory Space

The CX25800 registers and 32 kB SRAM are mapped into the 16 MB address space defined by each PCI function Base Address register. This means that the registers and SRAM can be accessed in the memory space of any function. The memory map in Table 9 indicates the 24-bit offset from the base address of the functions.

Table 9. CX25800 Memory Space

Beginning Address	Resource
24'h000000	unused
24'h180000	SRAM (32 kB)
24'h188000	unused
24'h200000	DMAC
24'h310000	Video
24'h320000	Audio
24'h330000	Transport Stream
24'h340000	VIP
24'h350000	Miscellaneous
24'h360000	Two-Wire Serial Interface
24'h370000	unused
24'h380000	General Purpose Host
24'h3D0000	unused

2.4.9 PCI Data Streaming

The CX25800 uses the resources in the PCI Subsystem to stream data between its peripherals and the host processor, across the PCI bus. A total of 12 streams of data are supported, and can be active simultaneously, although the typical application scenario uses a subset of the streams. The streams are independent from each other and are controlled on an individual basis. There are two types of data stream channels: downstream and upstream. A downstream channel transfers data from a peripheral to the host memory using the PCI bus. An upstream channel transfers data from the host memory to a peripheral using the PCI bus. High performance internal data paths and programmable depth FIFOs are used to optimize the throughput of data across the PCI bus. The programmable depth FIFOs, which are implemented using the internal SRAM, decouple the constant rate flow of peripheral data from the bursts and latencies of the PCI bus. The channels have been assigned an arbitrary number that is used for identification. Table 10 lists the channel information.

Table 10. MA Channel Assignment

Channel Number	Purpose	Type	BW_{max} (MHz)
21	Video packed or planar Y (luminance)	down	48
22	Video planar U (chrominance)	down	6
23	Video planar V (chrominance)	down	6
24	Video VBI (vertical blanking interval data)	down	36
25	Audio	down	0.2
26	Audio (to digital-analog converters)	up	0.2
28	Transport Stream (MPEG)	down	9
29	VIP Host (from Video Interface Port peripheral)	down	6.5
30	VIP Host (to Video Interface Port peripheral)	up	6.5
31	GP Host (from General Purpose Host peripheral)	down	6.5
32	GP Host (to General Purpose Host peripheral)	up	6.5

2.4.10 SRAM

The CX25800 contains an internal 32 kB SRAM that is used to store data and control information for the active streams. The use of the SRAM is programmable to accommodate a wide range of application scenarios. For example, an application can implement larger FIFOs on high bandwidth streams and smaller FIFOs on low bandwidth streams to handle the transfer latencies that may be encountered on the PCI bus. A multiple stream application may have some streams that are more tolerant to occasional data loss than others. The more critical streams can use deeper FIFOs, while the more tolerant streams can use smaller FIFOs. In addition to the FIFOs, the SRAM is used for control information, namely, RISC instruction queues, Channel Management Data Structures (CMDS), and optionally RISC programs. For each application, the FIFO depth for each stream is programmable, with the obvious restriction that the SRAM space used for the FIFOs plus the control information for all the active streams, cannot exceed 32 kB.

2.4.11 FIFO Size Calculation

FIFOs are used to decouple the constant data rate stream and the burst transfer nature of the PCI bus. Although the PCI bus has sufficient average bandwidth to accommodate the demands of the peripherals, latencies can exist that are significant and can cause loss of peripheral data if no buffering is provided. The amount of FIFO buffering required depends on the average bandwidth of the peripheral data and the duration of PCI latencies to be tolerated. Latencies encountered on PC systems are usually in the 10–20 microsecond range, with occasionally longer latencies of 100–200 ms. By sizing the FIFO buffers properly, most applications are able to protect its streams from the PCI latencies that are commonly encountered. The amount of buffering is the multiplication product of the average bandwidth of the data stream and the PCI latency duration.

The following is an example calculation of the FIFO buffer required for a video PAL, 768 pixel x 576 lines, RGB16 stream to tolerate a 200 microsecond PCI latency. The data stream bandwidth would be 24 MBps (25 frames per second * 625 total lines per frame * 768 pixels per line * 2 bytes per pixel = 24 MBps). The amount of FIFO buffering required would be 4800 bytes (24 MBps * 200 ms = 4800 bytes). Since the FIFO buffer must be a multiple number of lines and be two or greater, the FIFO buffer would actually be 6144 bytes (4800 bytes / 2 bytes per pixel / 768 pixels per line = 3.125 lines, rounded up to 4 lines * 768 pixels per line * 2 bytes per pixel = 6144 bytes). The actual latency protection would be 256 ms (6144 bytes / 24 MBps = 256 ms). Rounding down to 3 lines would require only 4608 bytes (3 lines * 768 pixels per line * 2 bytes per pixel = 4608 bytes), which would provide latency protection of 192 ms (4608 / 24 MBps = 192 ms).

The following is an example calculation of the FIFO buffer required for an ATSC MPEG transport stream (2.5 MBps) to tolerate a 200 microsecond PCI latency. The artificial line length is arbitrary, and the value chosen affects the size of the FIFO as it must be a multiple number of lines. This example is done using an artificial line length of 4 MPEG packets, which is 752 bytes (4 packets * 188 bytes per packet). The amount of FIFO buffering required would be 500 bytes (2.5 MBps * 200 ms = 500 bytes). Since the FIFO buffer must be a multiple number of lines and must two or greater, the FIFO buffer would actually be 1504 bytes (752 bytes per line * 2 lines = 1504 bytes). The actual latency protection would be 601.6 ms (1504 bytes / 2.5 MBps = 601.6 ms).

2.4.12 Programmable FIFO

A programmable FIFO is implemented in the SRAM using a number of equal sized buffers, known as Cluster Buffers, and a table of pointers to the buffers, known as a Cluster Descriptor Table (CDT). The CDT table must be initialized before the APB DMAC CNT2 register is initialized, and before the FIFO_EN bit is set to 1. In addition, PTR2 and CNT1 must be initialized before the FIFO_EN bit is set to 1. The number of buffers and the size of the buffers are programmable, and are chosen based on the depth of the FIFO needed. For example, if a 1 kB FIFO is needed for a stream, it could be implemented using 4, 256 byte buffers. A different stream could have a 1 kB FIFO implemented using 8, 128 byte buffers.

Although the number and size of the buffers are programmable, there are a few restrictions. The number of buffers must be two or greater. This allows the peripheral to be streaming data to or from a buffer, while the PCI DMA controller bursts data to or from a different buffer. Each buffer must large enough to accommodate one and only one line of peripheral data, and be an integer number of qwords (8 bytes). For video streams, the line size is dependent on the video format. For example, a 768 pixel x

576 line, RGB32 format would have 3 kB lines. The other downstream peripherals are not inherently line based and therefore use an artificial line length chosen by the application. For example, an MPEG Transport Stream may chose a line length equal to four packets, which would be 752 bytes (4x 188 bytes).

To specify the buffer size, use the DMAx_CNT1 register, where x is the number of the stream from Table 2-6. The register is written with the number of qwords minus one. For example, to specify 3 kB as the size of the buffers for the packed video stream, write 11'h17F to the DMA21_CNT1 register. To specify the buffer locations, use the CDT as described in the following paragraphs.

The set of buffers that make up a FIFO are supported by a CDT, which is also located in the SRAM. The table contains a four-dword descriptor for each buffer; therefore, the size of the CDT is directly related to the number of buffers that make up the FIFO. For example, a FIFO that was made up of three buffers would have a three entry table which would be a total of 48 bytes. The first dword of each entry is the address of the beginning of the buffer. The address is a 24-bit SRAM address (24'h18xxxx) and must be dword aligned. The other three dwords of each descriptor are reserved for use by the internal hardware.

To specify the CDT size, use the DMAx_CNT2 register, where x is the number of the stream from Table 2-6. The register is written with the number of qwords. For example, to specify 48 bytes as the size of the CDT for the packed video stream, write 11'h006 to the DMA21_CNT2 register. This value must also be written to the CDT Size field in the Channel Management Data Structure (CMDS).

To specify the SRAM location of the CDT, use the DMAx_PTR2 register, where x is the number of the stream from Table 2-6. The register is written with the 24-bit SRAM address (24'h18xxxx) and must be dword aligned. For example, to specify 15'h1000 as the CDT location for the packed video stream, write 24'h181000 to the DMA21_PTR2 register. This value must also be written to the CDT Base field in the Channel Management Data Structure (CMDS).

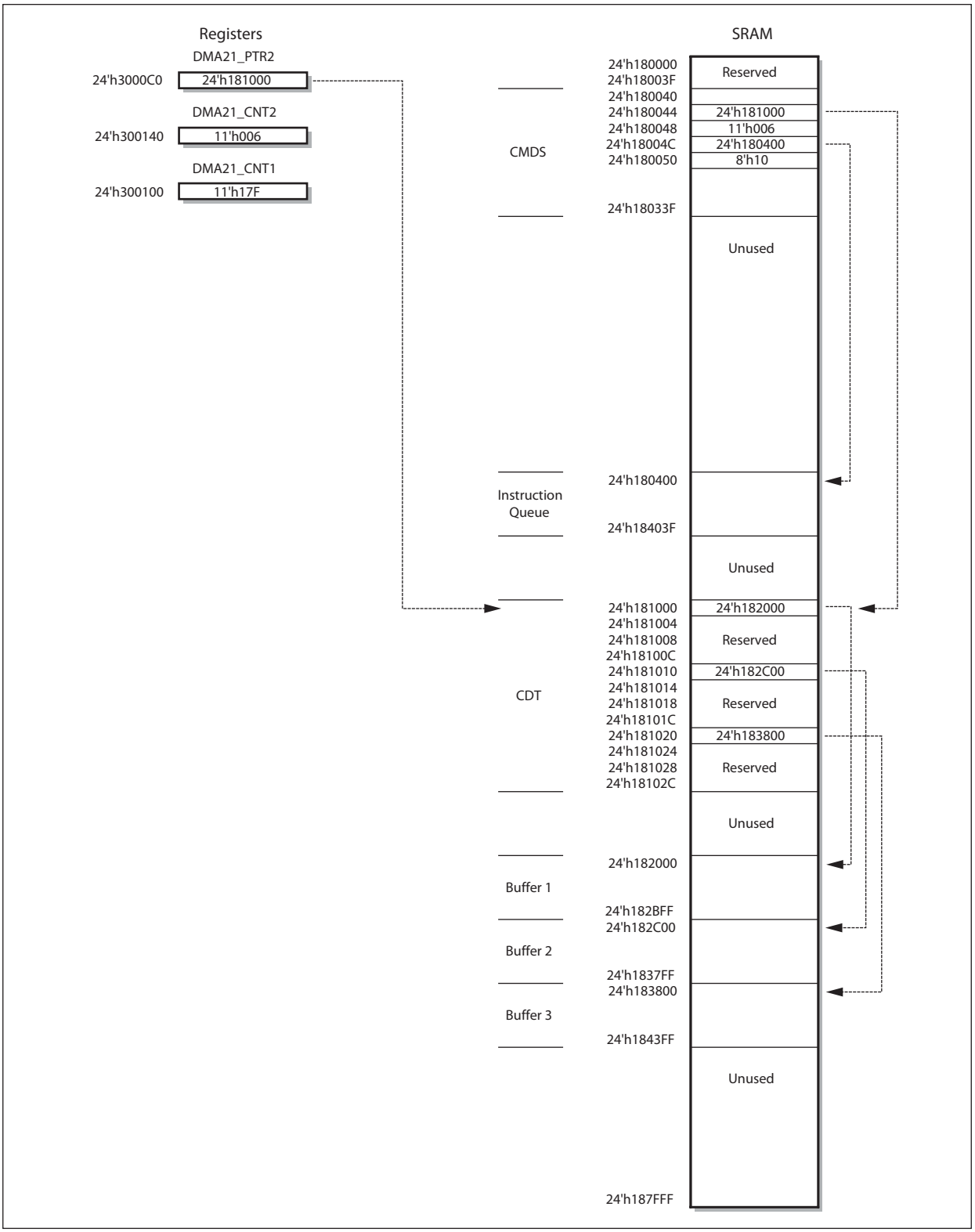
To specify the SRAM locations of the buffers, use the first dword of each descriptor in the CDT. The register is written with the 24-bit SRAM address (24'h18xxxx) and must be dword aligned. For example, to specify the SRAM locations for the start of three, 3 kB buffers to be 15'h2000, 15'h2C00, and 15'h3800, using a CDT that is located at 15'h1000, write 24'h182000 to 24'h181000, 24'h182C00 to 24'h181010, and 24'h183800 to 24'h181020.

The CDT and buffers can be located anywhere in the SRAM with the exception of the address range 15'h0000 to 15'h033F, which is reserved for the Channel Management Data Structures.

2.4.13 RISC Instruction Queue

The CX25800 DMA architecture includes a RISC controller, which is programmed using a simple set of RISC instructions. A series of RISC instructions form a program that specifies the PCI target addresses and the amount of data to be read or written by the CX25800 DMA controller. The RISC programs are generated by the software driver on the host and are stored either in host memory or in CX25800 SRAM. A valid RISC program must be in place before the corresponding RISC_EN bit is set to 1. Each active stream implements a RISC instruction queue in the SRAM to maximize the flow of instructions from the program memory to the RISC controller. When the RISC controller has no other higher priority task to attend to, such as transferring stream data, it attempts to keep the instruction queue full. This increases the system performance as the RISC controller virtually always has the next instruction available in SRAM when it needs it, and does not have to wait until it can fetch it from the host memory. The instruction queues are programmable in size and location in the SRAM. The minimum size is 8 dwords, the maximum size is 255 dwords, and the typical size is 16 dwords. Use the Instruction Queue Base and Instruction Queue Size fields in the Channel Management Data Structure (CMDS) to specify the location and size. The address must be dword aligned, and the size is in dwords. For example, to specify the packed video instruction queue to be 16 dwords in size and begin at address 15'h0400 in the SRAM, write 24'h180400 to address 24'h18004C, and write 8'h10 to address 24'h180050. See Figure 24 for an example.

Figure 24. SRAM Resource Example



2.4.14 Channel Management Data Structure

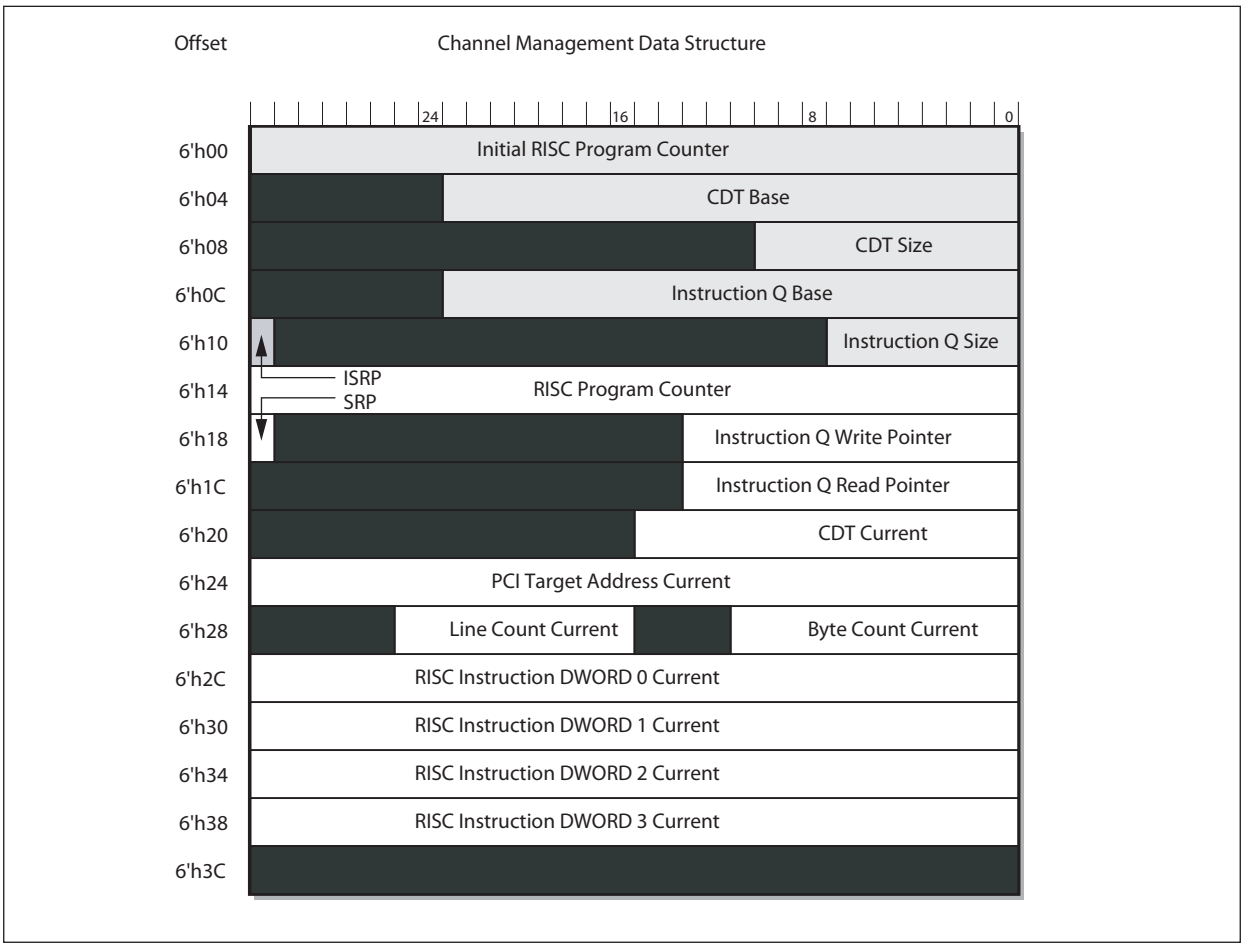
The CX25800 uses the SRAM to store information to manage each stream channel. This information is called the Channel Management Data Structure (CMDS) and is fixed in the SRAM from address 15'h0040 to 15'h033F. The CMDS for each channel is located in the SRAM as shown in Table 11.

Table 11. Channel Management Data Structure

Number	Purpose	CMDS Base
21	Video packed or planar Y (luminance)	15'h0040
22	Video planar U (chrominance)	15'h0080
23	Video planar V (chrominance)	15'h00C0
24	Video VBI (vertical blanking interval data)	15'h0100
25	Audio	15'h0140
26	Audio (to digital to analog converters)	15'h0180
28	Transport Stream (MPEG)	15'h0200
29	VIP Host (from Video Interface Port peripheral)	15'h0240
30	VIP Host (to Video Interface Port peripheral)	15'h0280
31	GP Host (from General Purpose Host peripheral)	15'h02C0
32	GP Host (to General Purpose Host peripheral)	15'h0300

The CMDS is composed of 16 dwords. The first five dwords (shown in gray in Figure 25) are information that is supplied by the host software to control and set up the RISC controller. The next ten dwords (shown in white in Figure 25) are used by the RISC controller to manage the stream channel. These fields are not to be written by the host software, although they can be read to monitor the channel information. The last dword (shown in black) is reserved and not used at this time, as are the rest of the fields shown in black in Figure 25. This figure also shows the layout of the CMDS. The fields of the CMDS are described in the next paragraph.

Figure 25. Channel Management Data Structure



Initial RISC Program Counter[31:0]

Location of the first RISC instruction. In SRAM Resident Program mode (SRP =1), this location is an SRAM address, and only bits [23:0] are relevant. In PCI Memory Resident Program mode (SRP = 0), it is a PCI target address of the host memory. The SRP bit is located at bit [31] in the dword at offset 6'h10.

CDT Base[23:0]

Location of beginning of the CDT in the SRAM. This address must match the address written to the DMAx_PTR2 register, where x is the number of the stream from Table 2-6. See the description of the CDT in the Programmable FIFOs section.

CDT Size[10:0]

The size in qwords of the CDT. This value must match the size written to the DMAx_CNT2 register, where x is the number of the stream from Table 2-6. See the description of the CDT in the Programmable FIFOs section.

Instruction Q Base[23:0]

Location of the beginning of the RISC instruction queue.

Instruction Q Size[7:0]

The size in dwords of the RISC instruction queue.

ISRP[31] (Initial SRAM Resident Program)

Used to specify whether the address in the Initial RISC Program Counter field is an SRAM address (ISRP =1), or a PCI target address (ISRP = 0).

RISC Program Counter[31:0]

The RISC controller uses this as temporary storage for the address of the current RISC instruction it is processing.

SRP[31] (SRAM Resident Program)

Used by the RISC controller to determine whether the program counter contains an SRAM address (SRP =1), or a PCI target address (SRP = 0).

Instruction Q Write Pointer[13:0]

Used by the RISC controller to maintain the location of the next dword to be written. This is a dword address, not a byte address.

Instruction Q Read Pointer[13:0]

Used by the RISC controller to maintain the location of the next dword to be read. This is a dword address, not a byte address.

CDT Current[15:0]

The RISC controller uses this as temporary storage for the current entry in the CDT that is being processed.

PCI Target Address Current[31:0]

The RISC controller uses this as temporary storage for the current PCI target address.

Byte Count Current[11:0]

The RISC controller uses this as temporary storage for the number of bytes of the current line that have been processed.

Line Count Current[25:16]

The RISC controller uses this as temporary storage for the current line it is processing.

RISC Instruction DWORD 0-3 Current[31:0]

The RISC controller uses this as temporary storage for the current instruction being processed.

2.4.15 RISC Controller

The CX25800 DMA architecture includes a RISC controller, which coordinates the transfer of data over the 12 stream channels. Although each channel has independent control and data buffering, they are all handled by the single RISC controller. The RISC controller is put into a reset state whenever the CX25800 is reset. To allow the RISC controller to operate the RUN_RISC bit[5] in the Device Control #2 register must be set to 1. The RISC controller can be returned to the reset state at any time by clearing the RUN_RISC bit to 0.

2.4.16 RISC Instructions

The RISC controller processes a program made up of a series of RISC instructions. The purpose of the RISC program is to specify the PCI target addresses and the amount of data to be read or written by the CX25800 DMA controller. The RISC programs are generated by the software driver on the host and are stored either in host memory or in CX25800 SRAM. The address of the beginning of the program must be written to the Initial RISC Program Counter field in the CMDS. When the channel is turned on, the RISC controller loads the initial program counter into the program counter and begin processing the instructions. Programs that are stored in the host memory are called PCI Memory Resident Programs, while programs that are stored in the CX25800 SRAM are called SRAM Resident Programs. To indicate whether the address in the Initial RISC Program Counter is a PCI memory address or a CX25800 SRAM address, the Initial SRAM Resident Program (ISRP) bit must be written. The ISRP bit is bit [31] at offset 6'h10 in the CMDS. A PCI Memory Resident Program is specified by writing the ISRP bit to 0, an SRAM Resident Program is specified by writing the ISRP bit to 1. See Figure 2-11, Channel Management Data Structure.

The RISC instruction set is composed of 10 instructions that can be categorized as downstream, upstream, and common to both directions. The downstream instructions are SYNC, WRITE, and WRITEC. The upstream instructions are READ and READC. The instructions that can be used in both downstream and upstream programs are JUMP, SKIP, WRITERM, WRITECM, and WRITECR. See Figure 26 through 2-21 for RISC instruction specifics.

Figure 26. SYNC Downstream RISC Instruction

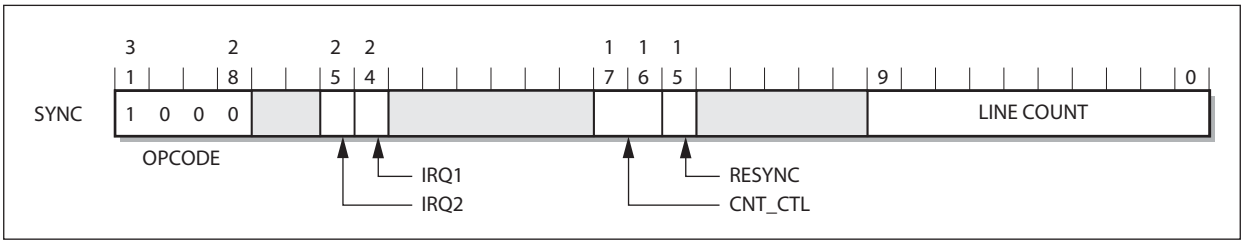


Figure 27. WRITE Downstream RISC Instruction

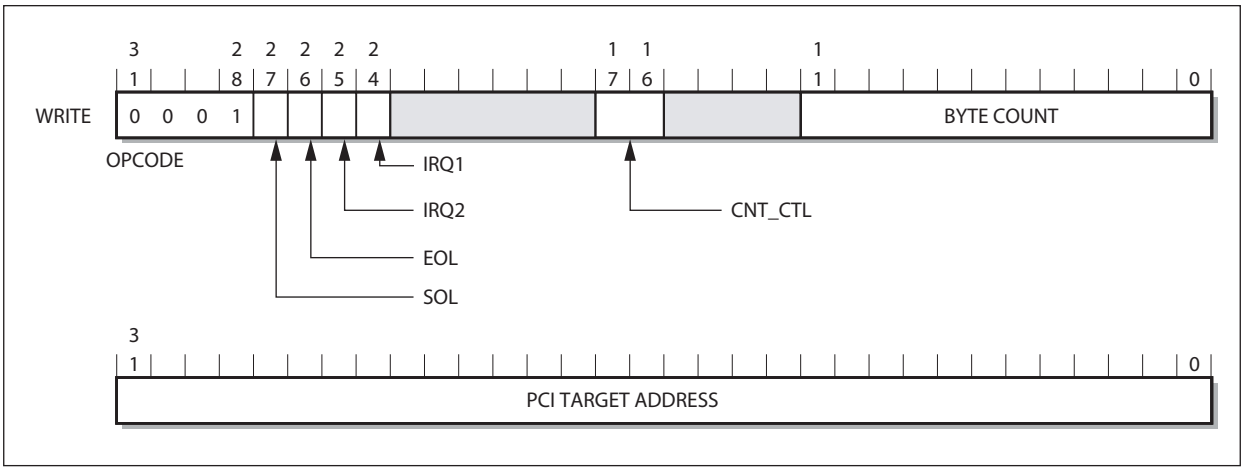


Figure 28. WRITEC Downstream RISC Instruction

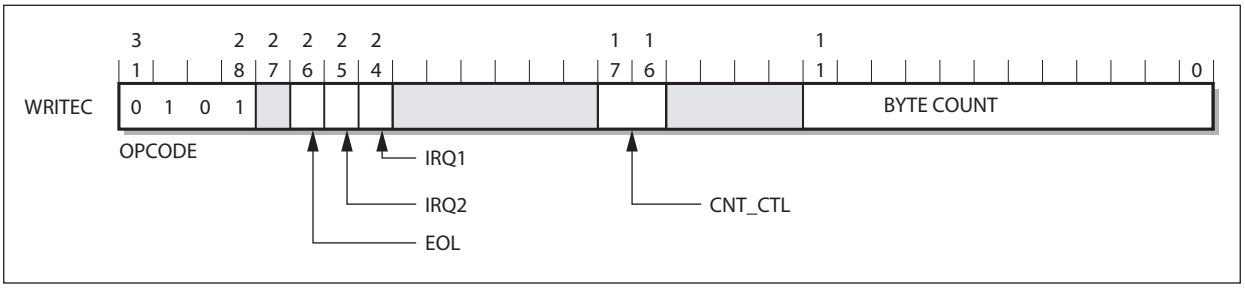


Figure 29. READ Upstream RISC Instruction

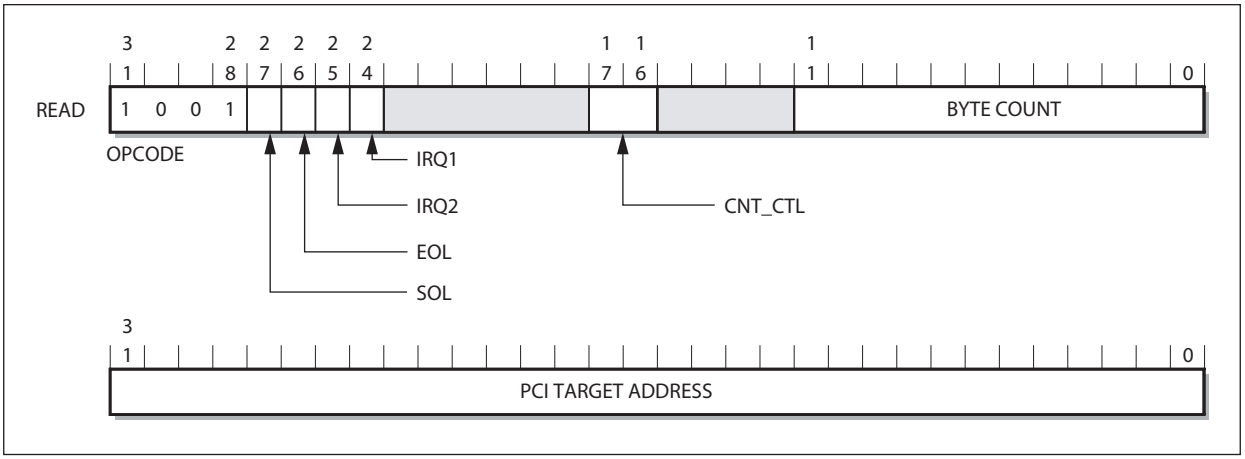


Figure 30. READC Upstream RISC Instruction

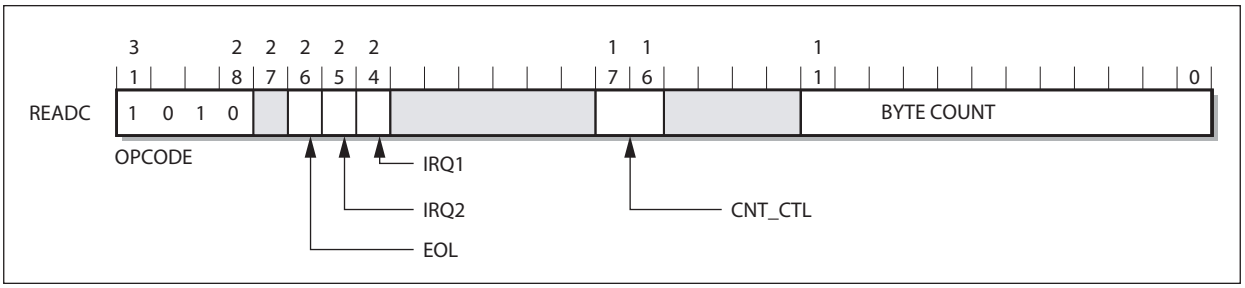


Figure 31. SKIP RISC Instruction

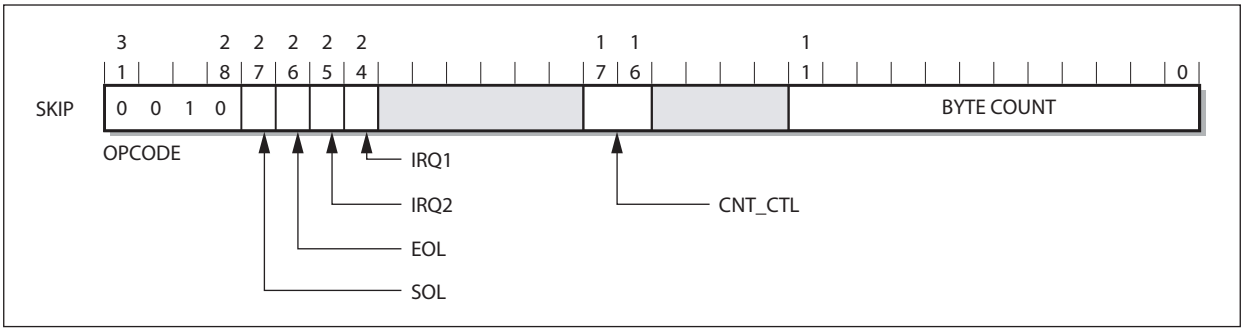


Figure 32. Jump RISC Instruction

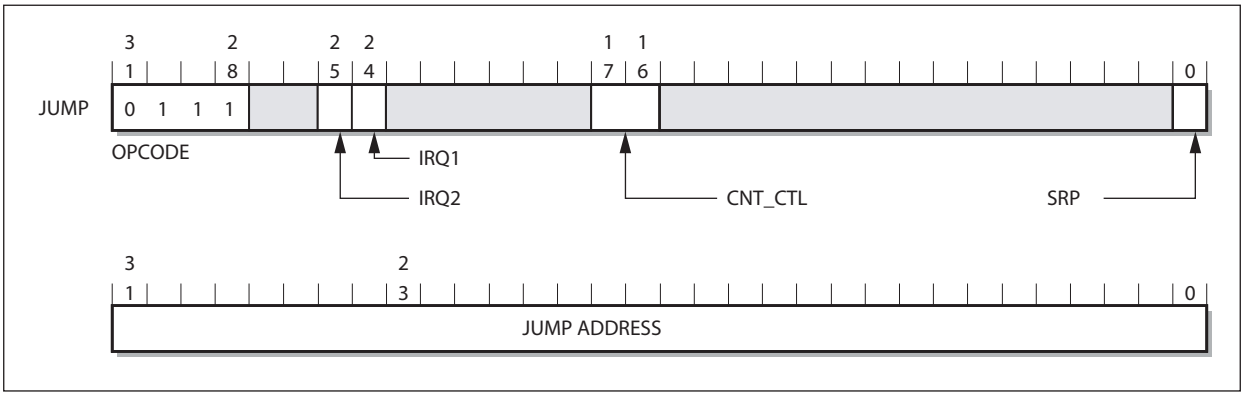


Figure 33. WRITERM RISC Instruction

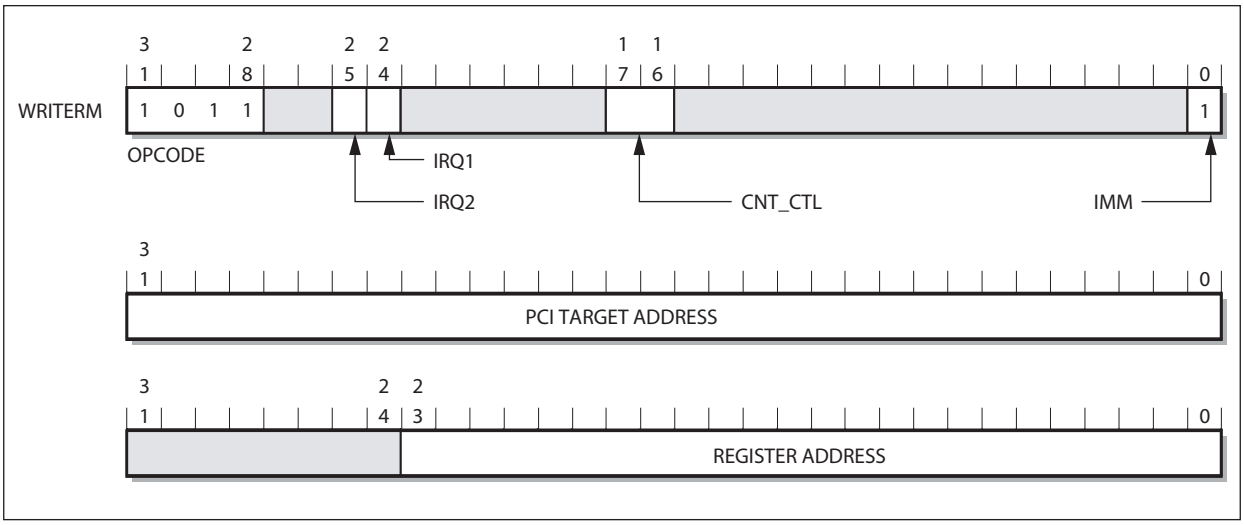


Figure 34. WRITECM RISC Instruction

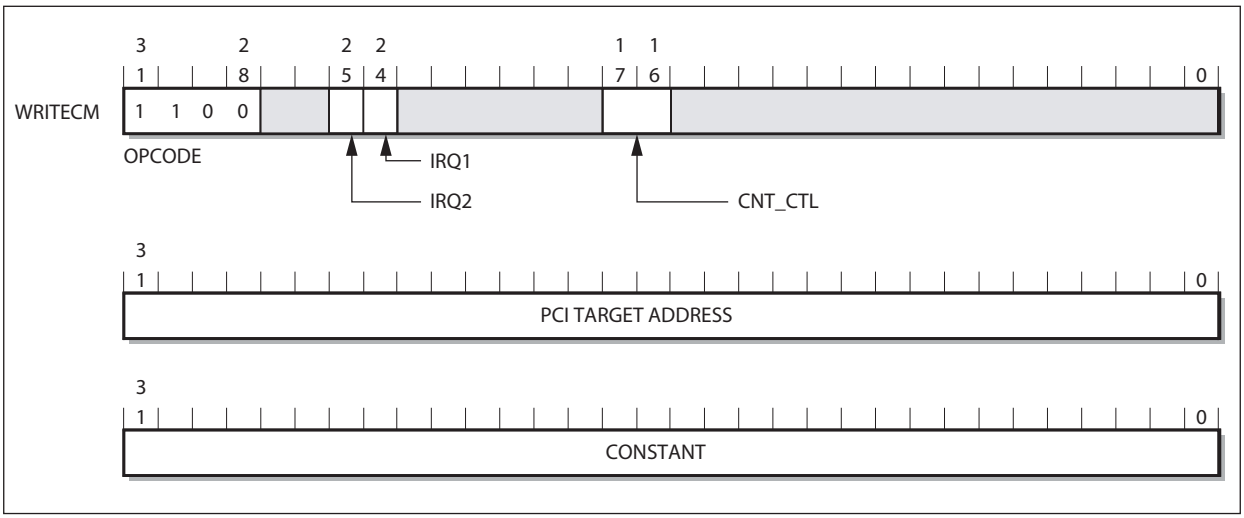
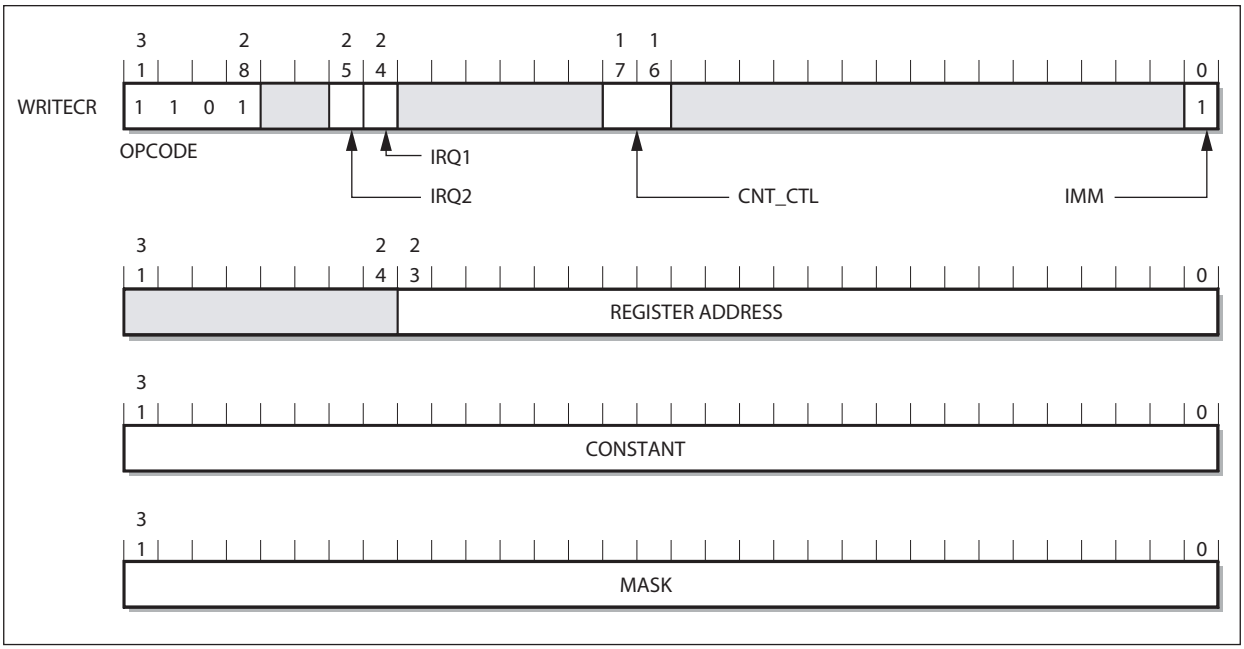


Figure 35. WRITECR RISC Instruction



All instructions contain two interrupt bits, IRQ1 and IRQ2, that can be used to set the RISCI1 and RISCI2 bits respectively, in the interrupt status register of the corresponding function. This allows a PCI interrupt to be generated when the instruction is executed by the RISC controller. All instructions have control bits for the general purpose counter associated with each channel. This allows the software driver to count RISC program events. The two bit CNT_CTL field is coded for the following action: 2'b00 = no change, 2'b01 = increment, 2'b10 = reserved, 2'b11 = reset to 0.

SYNC is a one-dword instruction as shown above. It is used only in downstream channels to specify which line to synchronize to. This is especially important for the video streams, which are by nature line based. The lines of the odd video field are numbered starting at 10'h000, while the lines of the even video field are numbered starting at 10'h200. The other downstream channels are not naturally line based, and therefore use artificial lines. Each downstream channel has a line length register to program the number of bytes in each line. Typically, the streams that have artificial lines use a SYNC to line 10'h000 instruction.

The RISC controller discards the data of all lines until it encounters the line specified in the SYNC instruction. The SYNC instruction is then complete, and the next instruction is processed. If the RESYNC bit is 0, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel. If the RESYNC bit is 1, the interrupt bit is not set.

WRITE is a two-dword instruction, as shown above. It is used only in downstream channels to specify the number of bytes of the current line to transfer, and the PCI target address to which the data must be written. The WRITE instruction is used to write an entire line or a portion of a line. It cannot be used to write multiple lines. The SOL (start of line) and EOL (end of line) bits are used to specify the portion of the current line to be processed by the instruction. The SOL bit must be set when the instruction applies to the beginning of the line (i.e., no portion of the line has been transferred or discarded by the previous instruction). The EOL bit must be set when the instruction applies to the end of the line (i.e., all data of the line has been transferred). See Table 12 for the possible combinations. If these bits do not match the

expectations of the RISC controller, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel.

Table 12. SOL/EOL Combinations

SOL	EOL	Usage
1	0	A beginning portion of the line.
0	0	A middle portion of the line.
0	1	An ending portion of the line.
1	1	The entire line.

WRITEC is a one-dword instruction, as shown above. It is used only in downstream channels to continue the processing of a line that has been started by a previous WRITE or SKIP. The data is written to the PCI target address that immediately follows the last address accessed by the previous WRITE or SKIP. The WRITEC instruction can also follow other WRITEC or SKIP instructions. There is no SOL bit, as WRITEC cannot be used to transfer the beginning of a line. The EOL bit must be set when the instruction applies to the end of the line (i.e., all data of the line has been transferred). See Table 2-8 for the possible combinations. If this bit does not match the expectations of the RISC controller, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel.

READ is a two-dword instruction as shown above. It is used only in upstream channels to specify the number of bytes of the current line to transfer, and the PCI target address to which the data must be read. The READ instruction is used to read an entire line or a portion of a line. It cannot be used to read multiple lines. The SOL (start of line) and EOL (end of line) bits are used to specify the portion of the current line to be processed by the instruction. The SOL bit must be set when the instruction applies to the beginning of the line (i.e., no portion of the line has been transferred or discarded by the previous instruction). The EOL bit must be set when the instruction applies to the end of the line (i.e., all data of the line has been transferred). See Table 2-8 for the possible combinations. If these bits do not match the expectations of the RISC controller, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel.

READC is a one-dword instruction, as shown above. It is used only in upstream channels to continue the processing of a line that has been started by a previous READ or SKIP. The data is read from the PCI target address that immediately follows the last address accessed by the previous READ or SKIP. The READC instruction can also follow other READC or SKIP instructions. There is no SOL bit, as READC cannot be used to transfer the beginning of a line. The EOL bit must be set when the instruction applies to the end of the line (i.e., all data of the line has been transferred). See Table 2-8 for the possible combinations. If this bit does not match the expectations of the RISC controller, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel.

SKIP is a one-dword instruction, as shown above. It is used both in downstream and upstream channels to specify the number of bytes of the current line to discard. The data is discarded beginning at the PCI target address that immediately follows the last address accessed by the previous instruction. The PCI target address is advanced by the number of bytes in the instruction. The SKIP instruction is used to discard an entire line or a portion of a line. It cannot be used to discard multiple lines. The SOL (start of line) and EOL (end of line) bits are used to specify the portion of the current line to be

processed by the instruction. The SOL bit must be set when the instruction applies to the beginning of the line (i.e., no portion of the line has been transferred or discarded by the previous instruction). The EOL bit must be set when the instruction applies to the end of the line (i.e., all data of the line has been transferred). See Table 2-8 for the possible combinations. If these bits do not match the expectations of the RISC controller, the x_SYNC bit in the interrupt status register of the corresponding function is set, where x is the associated channel.

JUMP is a two-dword instruction, as shown above. It is used both in downstream and upstream channels to load the current program counter with the specified address. The jump address can be either an SRAM address (SRP = 1) in which case only address bits [23:0] are relevant, or a PCI target address (SRP = 0) in which case all 32 address bits are used.

WRITERM is a three-dword instruction, as shown above. It is used both in downstream and upstream channels to write the value of a CX25800 register specified by the address field to the PCI target address. This instruction is typically used as a debug tool, but may be found to useful in some special situations. The only registers that can be used with WRITERM are the ones referred to as immediate, which are shown in Table 13. The IMM bit must always be set to 1.

Table 13. WRITERM Registers

Address Range	Resource
24'h18xxxx	SRAM
24'h20xxxx	Miscellaneous registers
24'h30xxxx	Miscellaneous registers
24'h31Cxxx	Video registers
24'h32Cxxx	Audio registers
24'h33Cxxx	Transport Stream registers
24'h34Cxxx	Video Interface Port Host registers
24'h35xxxx	Miscellaneous registers
24'h38Cxxx	General Purpose Host registers

WRITECM is a three-dword instruction, as shown in Figure 2-20. It is used both in downstream and upstream channels to write a 32-bit constant value to the PCI target address. This instruction is typically used as a debug tool, but may be found to useful in some special situations.

WRITECR is a four-dword instruction, as shown above. It is used both in downstream and upstream channels to write a 32-bit constant value to a CX25800 register specified by the address field according to the specified mask. A 1 in any bit position of the mask field causes the corresponding bit in the constant field to be written to the specified register. A 0 in any bit position of the mask field causes the corresponding bit in the register to be left unchanged. This instruction is typically used as a debug tool, but may be found to useful in some special situations. It is often used to turn on the FIFO enable bit of an upstream channel after the FIFO has been filled by previous READ instructions. The only registers that can be used with WRITECR are the ones referred to as immediate, which are shown in Table 2-9. The IMM bit must always be set to 1.

2.4.17 Data Stream Control

Each of the 12 stream channels has a RISC_EN bit to control whether the RISC controller is actively processing the stream of data. The RISC_EN bit is located in the Streaming Enable register of the VIP and general purpose host functions, and in the DMA Control register of the video, audio, and transport stream functions. This bit is used to turn on the streaming of a channel after it has been configured (i.e., FIFO, RISC instruction queue, CMDS, RISC program, peripheral specific setup). This bit is used to turn off the streaming of a channel at any time by clearing it to 0.

Each of the 12 stream channels has a FIFO_EN bit to control whether the peripheral is actively storing data to the FIFO (in the case of a downstream channel) or taking data from the FIFO (in the case of an upstream channel). The FIFO_EN bit is located in the Streaming Enable register of the VIP and general purpose host functions, and in the DMA Control register of the video, audio, and transport stream functions.

In the downstream channels, the FIFO_EN bit is typically turned on at the same time as the RISC_EN bit, as they are in the same register. A valid RISC program must be in place before the corresponding RISC_EN bit is set to 1. In the upstream channels, the RISC_EN bit is typically turned on by the software driver writing the register, and the FIFO_EN bit is turned on by the upstream RISC program with a WRITECR instruction. This allows the RISC controller to fill the FIFO with data before the peripheral begins taking data from it.

2.4.18 Data Stream User Guide

The following is a description of the steps that must be taken to stream data using the CX25800. These steps are described in the following sections, and *must* be executed in the sequence listed below.

1. Initialize the CDT in SRAM.
2. Initialize the APB DMAC to use the CDT.
3. Build the RISC program in PCI memory or SRAM.
4. Initialize the Channel Management Data Structure in SRAM.
5. Enable the RISC controller.
6. Configure the peripheral.
7. Enable the peripheral.

Step 1: FIFO Buffer Size

Based on the bandwidth of the data stream and the PCI latency to tolerate, determine the amount of FIFO data buffering needed. Then based on the line size of the data stream, determine the number of cluster buffers are needed to provide the total data buffer requirement. This determines the number of entries needed in the CDT.

Step 2: CDT

Choose the locations for the cluster buffers in the SRAM and program the pointer to each using the first dword of each descriptor of the CDT. The remaining three dwords of each descriptor do not need to be initialized by the software, as the RISC controller initializes them upon being enabled. This table does not need to be reinitialized by the software when the data stream is disabled. The only time it must be changed is when the cluster buffers need to move, or additional entries are desired in the table.

Step 3: Cluster Buffer Size

Based on the line size of the data stream (from video format or artificial) specify the cluster buffer size in qwords using the DMAx_CNT1 register, where x is the number of the stream from Table 2-6. This register does not need to be reinitialized by the software when the data stream is disabled. The only time it needs to change is when the cluster buffers size needs to change.

Step 4: CDT Location and Size

Specify the SRAM location of the CDT using the DMAx_PTR2 register, where x is the number of the stream from Table 2-6. Based on the number of entries in the CDT, specify its size in qwords using the DMAx_CNT2 register, where x is the number of the stream from Table 2-6. These registers must be reinitialized by the software before the data stream is enabled.

NOTE: Writing DMA{x}_CNT2 registers (location 24'h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.

Step 5: RISC Program

Place the RISC program into PCI memory or SRAM depending on where it is to reside. The RISC program can reside in noncontiguous blocks of memory, with the JUMP instruction used to load the program counter with the address of the beginning of the next block.

Step 6: Channel Management Data Structure (CMDS)

Write the address of the beginning of the RISC program in the Initial RISC Program Counter field. Depending on whether the program resides in PCI memory or SRAM, write the ISRP bit.

Write the CDT Base and Size with the same values written to the DMAx_PTR2 and DMAx_CNT2 registers, respectively.

Decide the size and location in the SRAM of the RISC instruction queue. Write the Instruction Q Base and Size with the respective values. The size value is expressed in dwords. A size of 16 dwords is typical.

These fields do not need to be reinitialized by the software when the data stream is disabled.

Step 7: Configure Peripheral

Program any downstream line length register.

Program any other configuration registers specific to the operation of the peripheral.

Clear the interrupt status register and set the interrupt mask register of the function (video, audio, MPEG transport stream, VIP, general purpose host).

Set the mask of the PCI interrupt register.

Step 8: Enable RISC Controller

The RISC controller is held in a reset state by default after the CX25800 has been reset. Enable it to run by setting the RUN_RISC bit[5] in the Device Control #2 register to 1. The RISC controller does not begin to execute instructions and process data stream until the RISC enable bit for the data stream is set to 1.

Step 9: Enable Peripheral Data Stream

Enable the RISC controller to begin executing instructions and processing the data stream by setting the RISC_EN bit to 1. The RISC_EN bit is located in the Streaming Enable register of the VIP and general purpose host functions, and in the DMA Control register of the video, audio, and transport stream functions.

Enable the downstream peripheral to begin storing data to the FIFO. This is done by setting the FIFO_EN bit to 1. This is typically done at the same time as the RISC_EN bit is done, as they are in the same register.

Upstream peripherals are typically enabled using a WRITECR RISC instruction to set the FIFO_EN bit to a 1. This allows the RISC controller to fill the FIFO with data, providing PCI latency protection, before the peripheral begins taking data from it.

2.4.19 PCI Master

The PCI master uses the cache line commands, Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple, when appropriate, if enabled by the Memory Write and Invalidate Enable bit in the PCI Configuration Space Command register.

The PCI master arbitrates between writing the downstream data and reading the upstream or RISC instruction data. The transfer in either direction continues until completion, and then switches to transfer in the other direction. An exception to this is if the target terminates with RETRY consecutively and reaches the retry limit value programmed into the DMA_RTRY_LMT field in the Device Control #1 register. When this occurs, the master switches to transfer in the other direction.

A small percentage of PCI core logic chip sets may start a bus transaction during the same cycle that GNT# is deasserted. This is not PCI 2.3 compliant. To ensure compatibility when using PCs with these PCI core logic chip sets, the EN_VSFX bit in the Device Control #1 register is provided. When in this mode, the GNT# is not passed to the CX25800 master unless its REQ# is asserted. This prevents a bus transaction from starting the same cycle as GNT# is deasserted. This also has the side effect of not being able to take advantage of bus parking, this lowering arbitration performance. The CX25800 software driver must query for these noncompliant chip sets, and set the EN_VSFX bit only if required.

2.5 MPEG Data Port

The CX25800 has a dedicated high-speed port to receive MPEG transport, elementary or program streams from digital television channel demodulators or video compressors/codecs. Using DMA, these streams are sent to the host for software-based decompression or storage.

2.5.1 Video Compressors/Codecs

Alternatively, this port can be used to transfer compressed MPEG II or MPEG IV streams from video compressors/codecs that support compressed data output over a non-CPU-based bus, where data is continuously output and is synchronized either to an output clock or a data valid signal. The MPEG data port can absorb data rates up to 80 Mbps without throttling.

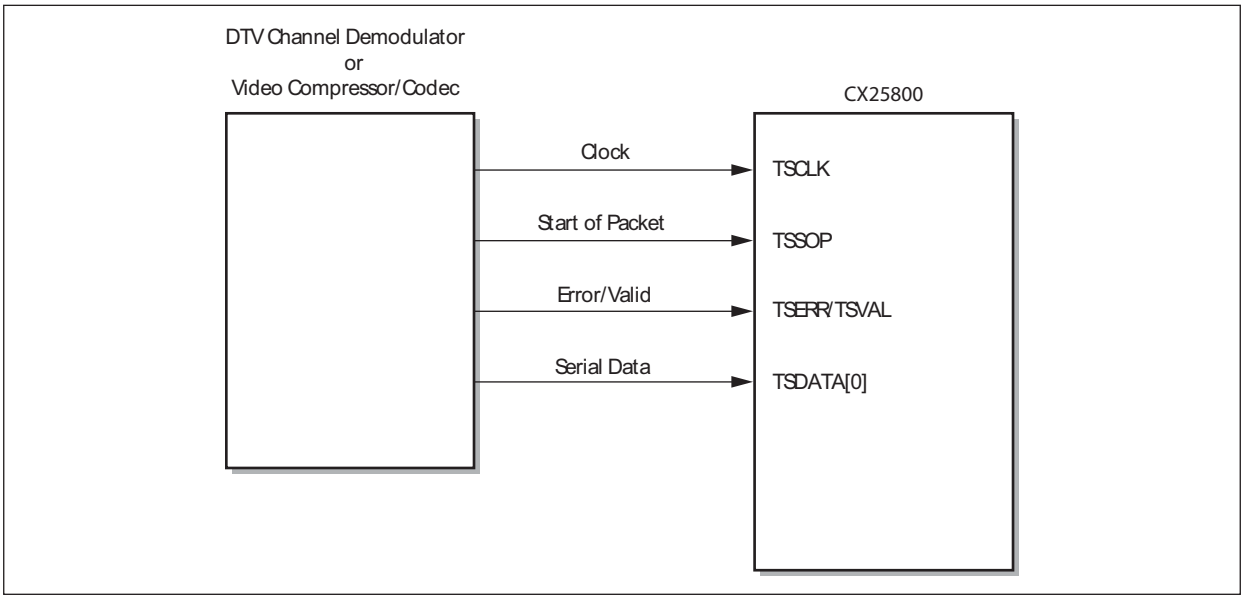
2.5.2 Serial vs. Parallel Interface

The MPEG data port can be configured for either a serial or parallel mode connection according to the functionality of the chosen channel demodulator or the video compressor/codec. Figure 36 illustrates the MPEG port serial interface.

If the channel demodulator or video compressor/codec supports both a serial and a parallel mode capability, the serial mode connection allows pins to be freed up and assigned as GPIO if desired.

NOTE: For very high-speed data applications (>40 Mbps), the parallel interface mode eases board layout concerns.

Figure 36. MPEG Port Serial Interface



2.5.3 MPEG ES (Elementary Stream)

Use Register IPB_AUTO_SOP in punctured clock mode to internally generate a start of packet for applications that have a continuous stream with no start of packet signal such as a MPEG elementary stream. This mode must be used with IPB_SOP_SEL set to 2'h3. Also, use IPB_CAP_ALL when doing elementary stream. IPB_CAP_ALL when set to 0, the SOP (first start of packet) is ignored to allow the logic to get reliably synchronized to the data stream. While discarding a packet of MPEG transport stream is not a problem, losing the beginning of an MPEG elementary stream can be a serious problem.

HW SOP Control (Immediate Access)

Register: HW_SOP_CONTROL

Location: 32'hE433C04C

Bits	Type	Default	Name	Description
[23:16]	RW	8'd47	IPB_STRT_BYTE	Byte start pattern that is searched for in the MPEG transport stream that signals start of transport stream. This is issued every mpeg packet.
[15:4]	RW	12'd188	IPB_PKT_LNGTH	Used to sync/mark detect SOP
[3]	RW	1'b0	IPB_ CAP_ALL	A value of 1 allows all data of a punctured clock stream to be captured. A value of 0 will result in the first two packets to be lost. This bit must only be set to 1 when in punctured clock mode.
[2]	RW	1'b0	IPB_ AUTO_SOP	A value of 1 eliminates the need for an external start of packet in punctured clock mode. It must only be used with IPB_SOP_SEL = 00. A value of 0 allows all other start of packet modes to be used.
[1:0]	RW	2'b00	IPB_STRT_FLTR_CNT	Defines the number of IPB_strt_bytes that need to be detected before the mpeg fec interface is declared as being in sync.

2.6 Video Decoder

This section describes the functionality of the analog video decoder in sequence from the video input at the analog front end to the output of digital video pixels from the pixel engine to the internal peripheral bus. For details of the analog front-end interfacing circuit to baseband video signals, see Chapter 3.

2.6.1 Video Input Multiplexer

The CX25800 has a 4:1 multiplexer that can be used to switch between four composite video sources. This multiplexer is controlled by the YADC_SEL bits 14 and 15 of the Input Format register.

Input Format Register

Register 24'h310104

Bits	Type	Default	Name	Description
[15:14]	RW	2'b00	YADC_SEL	Video input source selection. 00 = MUX1 01 = MUX2 10 = MUX3 11 = MUX4

2.6.2 10-bit Video Analog-to-Digital Converter

The CX25800 has a 10-bit, on-chip Analog-to-Digital Converter (ADC) to digitize incoming video baseband signals.

The ADC is used for digitizing composite video from video sources such as cameras with analog outputs.

2.6.3 Video Signal Locking

The line length (the interval between the midpoints of the falling edges of succeeding horizontal sync pulses) of analog video sources is not constant. For a stable source such as a studio quality source, test signal generator, or DVD player, this variation is very small (±2 ns). However, for an unstable source such as a VCR, the line length variation is as much as a few microseconds.

Digital display systems require a fixed number of pixels per line despite these variations. The CX25800 uses a technique known as UltraLock to lock to the horizontal sync and subcarrier of the desired analog video signal and generate the required number of pixels per line.

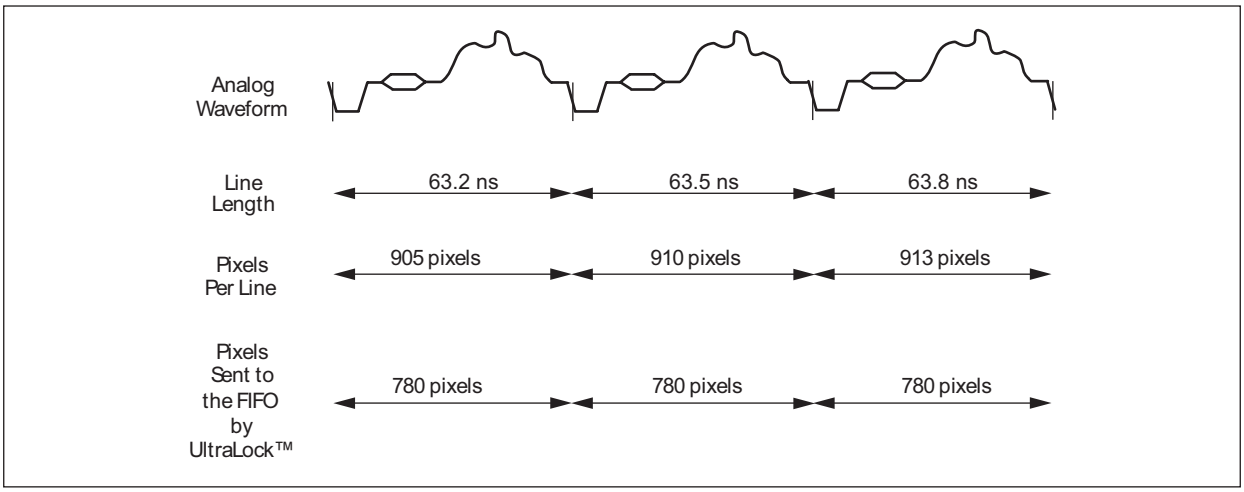
2.6.3.1 UltraLock Overview

UltraLock is based on video signal oversampling using a fixed-frequency, stable clock. Because the video line length varies, the number of samples generated using a fixed-frequency sample clock also varies from line to line. If the number of generated samples per line is always greater than the number of samples per line required by the particular video format, the number of acquired samples can be reduced to fit the required number of pixels per line.

UltraLock accommodates line length variations from nominal in the incoming video by always acquiring more samples than are required by the particular video format and outputting the correct number of pixels per line. UltraLock then interpolates the required number of pixels in a way that maintains the stability of the original image despite variation in the line length of the incoming analog waveform.

Figure 37 illustrates an example using 4 × Fsc sampling of three successive lines of video being decoded for square-pixel NTSC output. The first line is shorter than the nominal NTSC line time interval of 63.5 µs. On this line, a line time of 63.2 µs sampled at 4 × Fsc (14.31831 MHz) generates only 905 pixels. The second line matches the nominal line time of 63.5 µs and provides the expected 910 pixels. Finally, the third line is too long at 63.8 µs within which 913 pixels are generated. In all three cases, UltraLock outputs only 780 pixels.

Figure 37. UltraLock Behavior for NTSC Square Pixel Output using 4x Fsc Sampling Rate



UltraLock can be used to extract any programmable number of pixels from the original video stream as long as the sum of the nominal pixel line length (910 for NTSC and 1,135 for PAL) and the worst case line length validation from nominal in the active region is greater than or equal to the required number of output pixels per line:

$$P_{Nom} + P_{Var} \geq P_{Desired}$$

where: P_{Nom} = Nominal number of pixels per line at 4 × Fsc sample rate (910 for NTSC, 1,135 for PAL) *

P_{Var} = Variation of pixel count from nominal at 4 × Fsc (can be a positive or negative number)

$P_{Desired}$ = Desired number of output pixels per line

NOTE: Total number of pixels includes the active video region plus blanking and front porch.

2.6.4 Video Sample Rate Converter

2.6.4.1 Flexible Video Timing Formats

In the CX25800, the UltraLock circuit has been enhanced by a video sample rate converter. This capability is required for applications such as video editing/authoring and time shifting that require decoded video to be sent out of the CX25800 for compression and simultaneous direct connection to a digital video encoder.

In combination with UltraLock implemented in the video decoder, the sample rate converter allows a choice of video sampling rates and video decoding rates. This flexibility means that video can be captured at the highest possible sampling rate, using UltraLock, to acquire the maximum number of samples at the 10-bit ADCs).

If decoded video is required on the CX25800's output pixel port for connection of hardware MPEG compressors, TV encoders, or hardware video deinterlacers, the sample rate converter can be enabled to provide digital video with the following attributes:

- Provides a valid video data sample with each output clock
- Produces the same number of output clocks per line
- Generates consistent sample point locations from line-to-line

These attributes are mandatory for interfacing to the aforementioned devices.

Figure 38 provides a top level overview of the sample rate converter and video decoder.

Figure 38. UltraLock and Sample Rate Converter

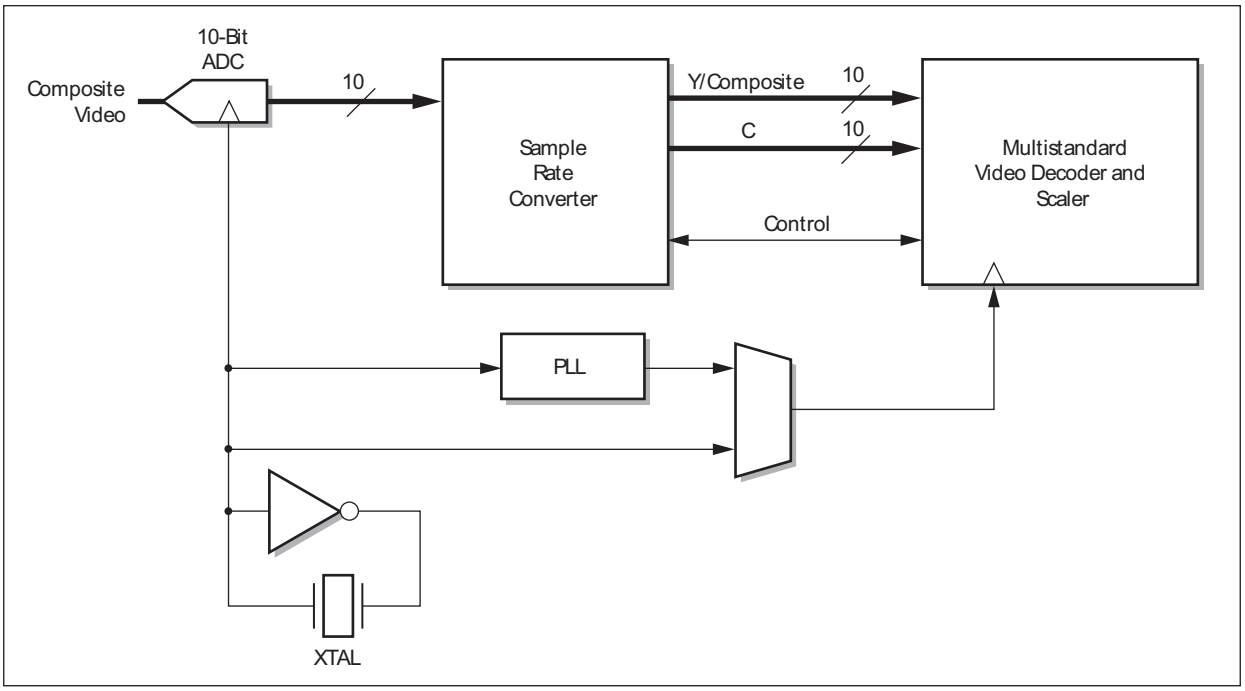


Figure 38 indicates that there is a clock domain for the analog to digital converters and another domain for the multistandard video decoder and scaler. Typically, an 8x Fsc (video subcarrier frequency) crystal is used to provide a sampling clock for the video ADCs to obtain more samples per line than is required (see UltraLock Overview) for square pixel or 4:3 aspect ratio decoding.

If no external video processing is required, the sample rate converter can be bypassed and the video decoder clocked at the same frequency as the ADCs. The decoded video samples are DMAd to the PCI bus and the graphics overlay surface in the same fashion as our previous video decoders.

If external video processing is required, the Sample Rate Conversion register should be programmed for the desired frequency of video decode. This is typically 27 MHz for ITU-R. BT656 decoding, although other formats such as square pixel NTSC (24.5454/12.2727 MHz) or PAL (29.5/14.75 MHz) may be supported. See Table 14.

Table 14. Video Decoding Formats

Video Standard	Parameter	601/656	Square Pixel
NTSC	Horizontal Pixels	720	640
	Vertical Lines	480	480
	Clock Rate	27 MHz	24.5454 MHz
PAL	Horizontal Pixels	720	768
	Vertical Lines	576	576
	Clock Rate	27 MHz	29.5 MHz

To use the Sample Rate Converter, the ratio between the ADC sampling frequency (typically 8x Fsc) and the desired Video decoder core frequency (typically 24.54, 27.0, or 29.5 MHz) must be derived, multiplied by 2^{17}, and converted to binary or hexadecimal.

Sample Rate Conversion Register

Register 24’h310170

Bits	Type	Default	Name	Description
[18]	RW	19'h21F07	SRC_REG_VAL	19-bit SRC programmable value. This is a ratio of the ADC clock rate to video clock rate. (ADC sampling frequency / Video decoder core frequency) * 2^{17}

Some examples of ADC sampling frequency versus desired video decoder frequency and the SRC value to be programmed are illustrated in Table 15.

Table 15. Sample Rate Conversion

XTAL Frequency (MHz)	Desired Video Decoding Frequency (MHz)	Application	SRC_REG_VAL (HEX)
28.636363	24.545454	Square Pixel NTSC	16'h23DF3
28.636363	27.000000	“601/656” NTSC/PAL	16'h21F07
28.636363	28.636363	8x Fsc NTSC	16'h20000
28.636363	29.500000	Square Pixel PAL	16'h1F102
28.636363	35.440000	8x Fsc PAL	16'h19D5F

2.6.5 Composite Video Input Formats

The CX25800 supports most video formats in use worldwide. Table 16 lists the video input formats supported by the CX25800 and some of the countries in which each format is used.

Table 16. Video Input Formats Supported by the CX25800

Format	Lines	Fields	Fsc (MHz)	Country
NTSC-M	525	60	3.58	U.S., many others
NTSC-Japan(1)	525	60	3.58	Japan
PAL-B, G, H	625	50	4.43	Western/Central Europe, others
PAL-D	625	50	4.43	China
PAL-I	625	50	4.43	U.K., Ireland, South Africa
PAL-M	525	60	3.58	Brazil
PAL-NC	625	50	3.58	Argentina
PAL-N	625	50	3.58	Paraguay, Uruguay

FOOTNOTES:
(1) NTSC—Japan has 0 IRE setup.

The video decoder must be programmed appropriately for each of the composite video input formats. Table 17 lists the register values that must be programmed for each input format.

Table 17. Register Values for Square Pixel Video Input Formats

Register	Bit	NTSC-M	NTSC-J	NTSC-4.43	PAL-B, D, G, H, I	PAL-M	PAL-N	PAL-NC	PAL-60
Input Format (24'h310104)	FMT[3:0]	0001	0010	0011	0100	0101	0110	0111	1000

2.6.6 Y/C Separation and Chroma Demodulation

2.6.6.1 The Y/C Separation Problem

Many video decoders employ a luminance notch filter, a chrominance band-pass filter, and a chrominance comb filter. The luminance signal is derived by filtering out the color information (chrominance) from a composite video signal with a notch filter. This works because the NTSC color information is in a frequency band centered at about 3.58 MHz that extends approximately. ±1.3 MHz (i.e., from 2.3 to 4.9 MHz). The Y filter rejects frequencies in that range. Although this effectively filters most of the chrominance signal out of the luminance signal, it also removes the higher frequency luminance signal components. This loss of bandwidth reduces the horizontal resolution of the luminance signal, and fine detail in the picture is lost. The chrominance signal is derived by band-pass filtering the composite video signal to extract the frequency band centered at 3.58 MHz that contains the color information. A chrominance comb filter removes any residual luminance (Y) signal that overlaps the chrominance (C) signal in this frequency range.

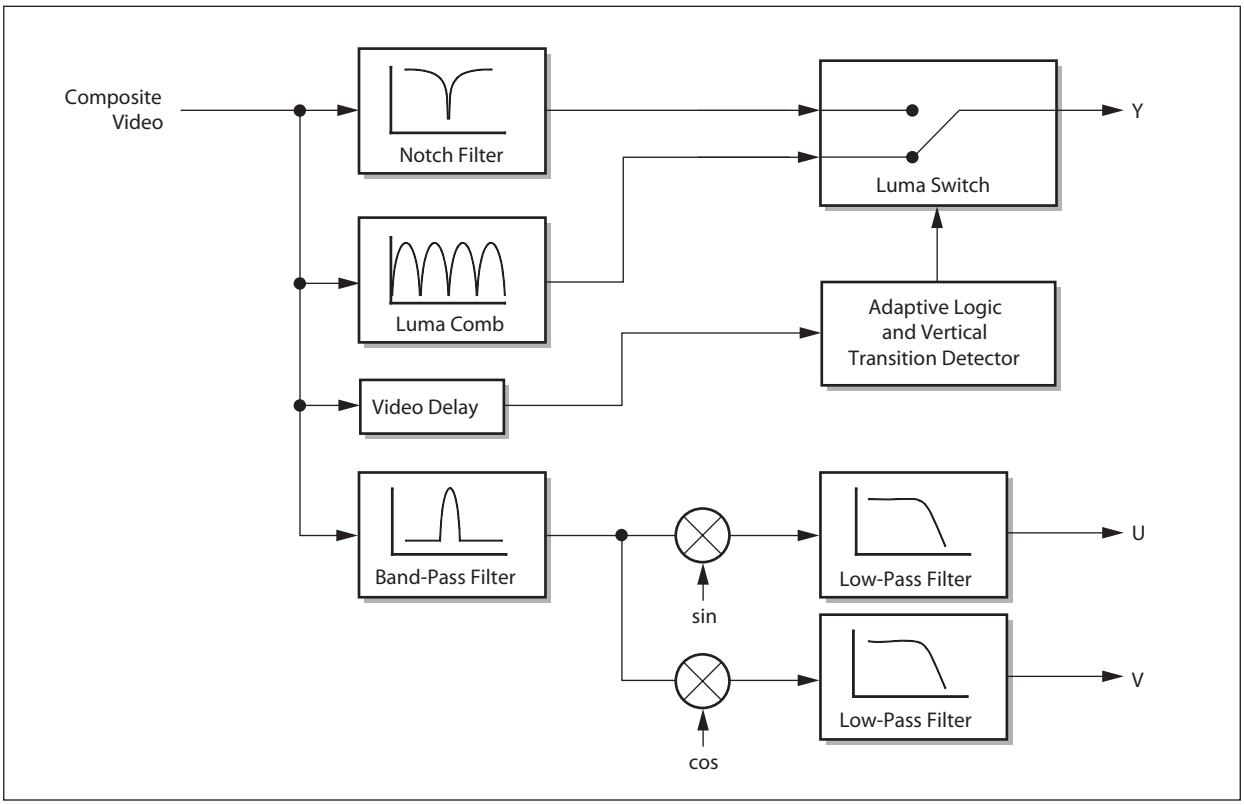
Other video decoders employ a line comb filter. These line comb filters operate by delaying the previous composite video horizontal scan line and comparing it to the current horizontal scan line. Adding the two lines together cancels the C signal and provides the Y signal. Subtracting the current line from the delayed line provides the C signal. This process creates two filters which have a frequency response that look like teeth in a comb. This type of filter is usually known as a 1-H comb filter, since it uses a 1-horizontal scan line delay to process the signals. More complex 2-H comb filters can be built using 2-horizontal scan line delays. While these filters show improvement with a multiburst test pattern compared to a notch filter and demonstrate a horizontal flat frequency response, the multiburst pattern does not show that
50 percent of the vertical resolution is lost due to the averaging of two lines. These filters still suffer the hanging dot problem noticeable on test patterns such as the SMPTE color bar test pattern.

2.6.6.2 Conexant Adaptive Comb Filter

To overcome this hanging dot problem and the loss of vertical resolution, a sophisticated 3-line, adaptive comb filter has been implemented in the CX25800 to separate the Y/C components in composite NTSC/PAL video signals. As stated previously, simple 1-H comb filters cannot eliminate hanging dots on a vertical color transition. Comb filtering two successive scan lines with different color values at the same horizontal positions along the lines cause the problem. The line comb filter cannot separate the Y/C signals correctly in this situation. The color signal crosses over into the luminance signal, creating a cross-luminance artifact. In a 3-line adaptive Y/C separation filter, adaptive logic continuously evaluates the video image and then selects the most efficient processing algorithm available in the filter. This is sometimes called a 2-D filter, because both the horizontal scan lines and vertical transitions are processed. This eliminates the hanging dot problem by detecting vertical transitions in the image.

The adaptation logic examines three successive horizontal scan lines simultaneously. If a vertical transition occurs between the first and third lines, notch filtered luminance and band-pass filtered chrominance are used directly, without comb filtering. Hence, two lines with different colors are not input to the comb filter at a transition boundary. Therefore, the Y/C signals are fully separated and the hanging dots eliminated. The CX25800 accomplishes this adaptive processing on a pixel-by-pixel basis, compared to other decoders which can only comb filter on a line by line basis. Figure 39 illustrates a high-level diagram of the NTSC/PAL adaptive comb filter.

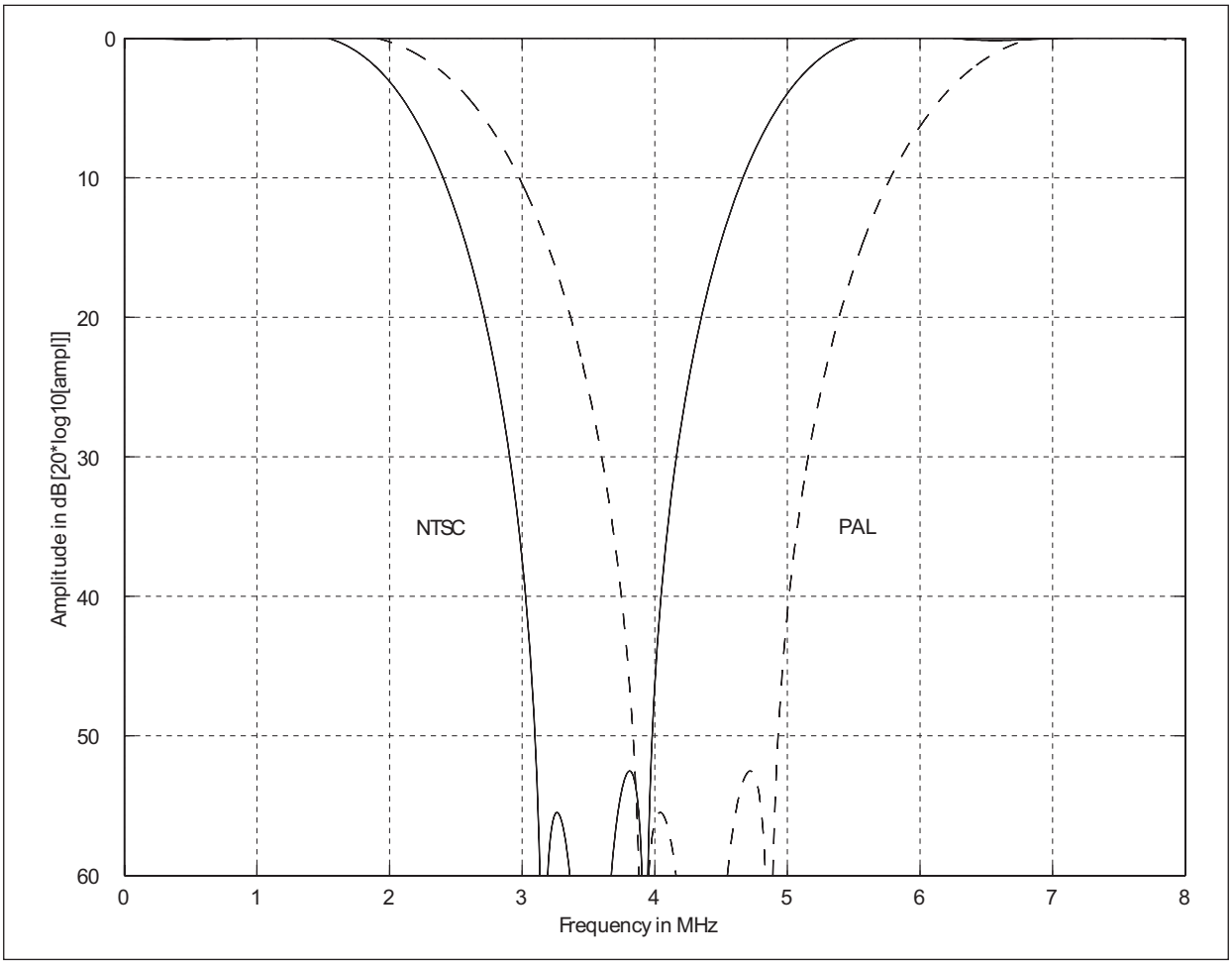
Figure 39. Y/C Separation and Chroma Demodulation Circuit for Composite NTSC/PAL Video



2.6.7 Y/C Separation and Chroma Demodulation

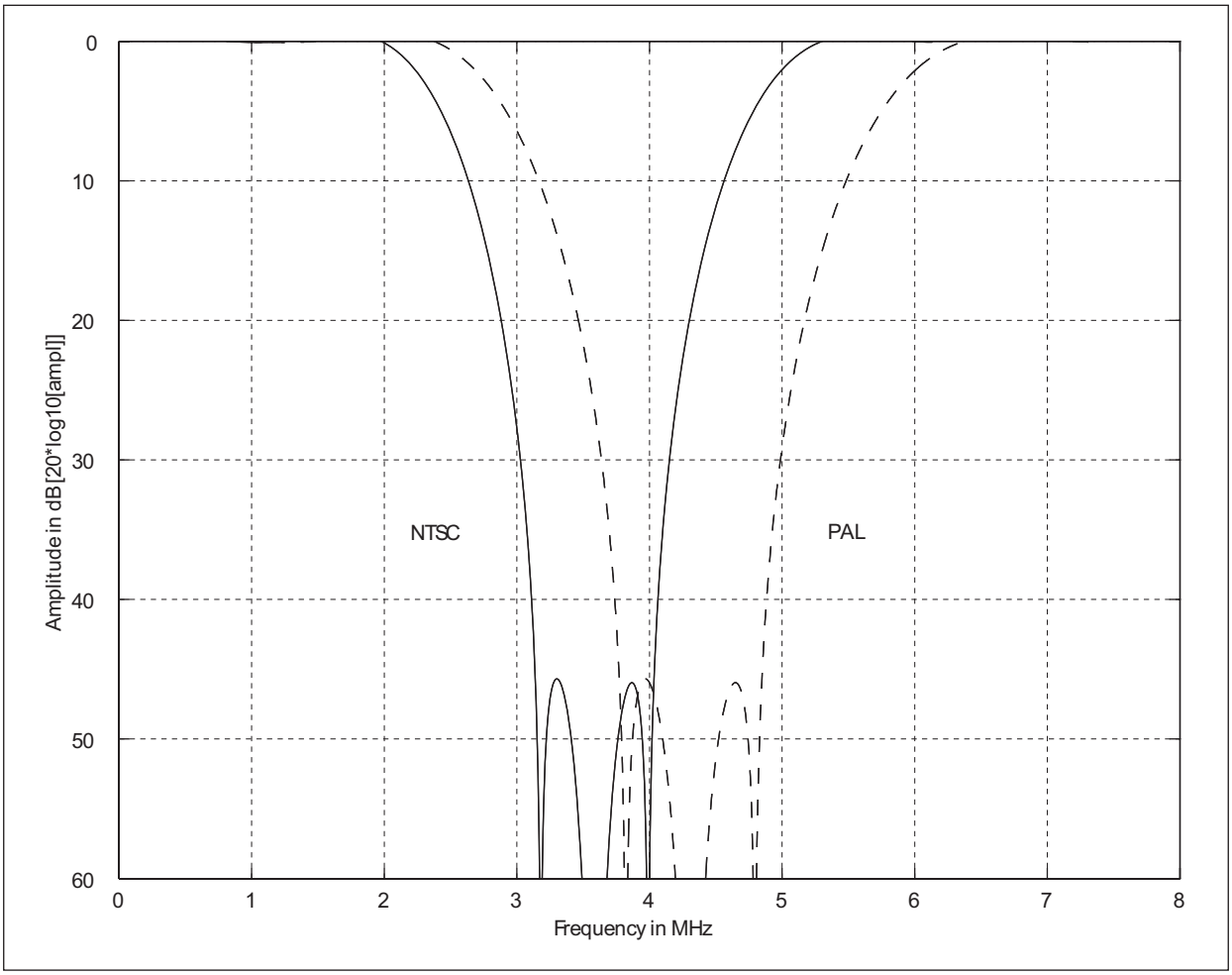
The luma notch filter responses for NTSC and PAL video, using 4x Fsc decoding (Y comb filter disabled) is illustrated in Figure 40.

Figure 40. Luma Notch Filter Frequency Responses for NTSC and PAL @ 4x Fsc Decoding Frequencies



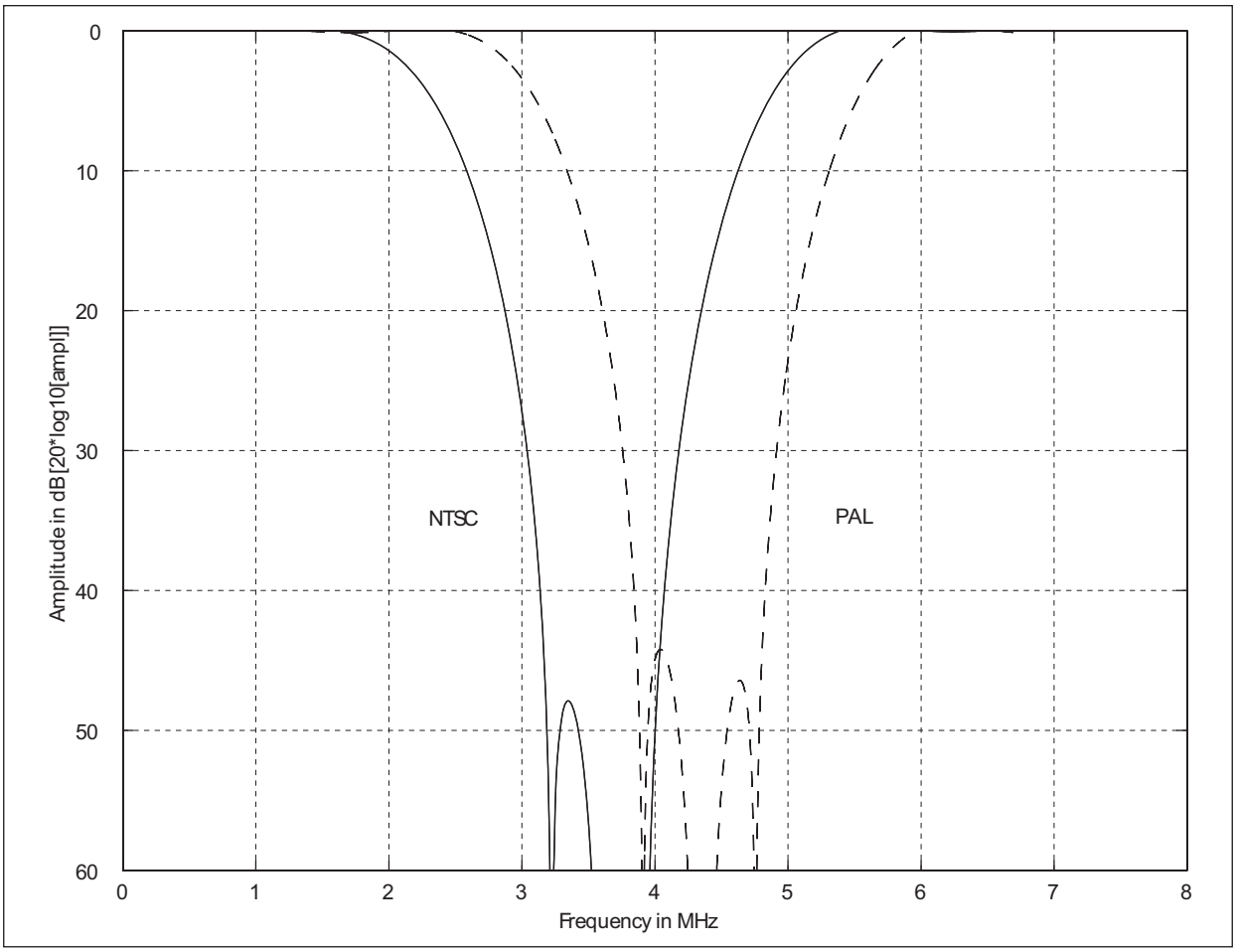
The luma notch filter response for NTSC and PAL video using square pixel decoding (Y comb filter disabled) is illustrated in Figure 41.

Figure 41. Luma Notch Filter Frequency Responses for NTSC and PAL @ Square Pixel Decoding Frequencies



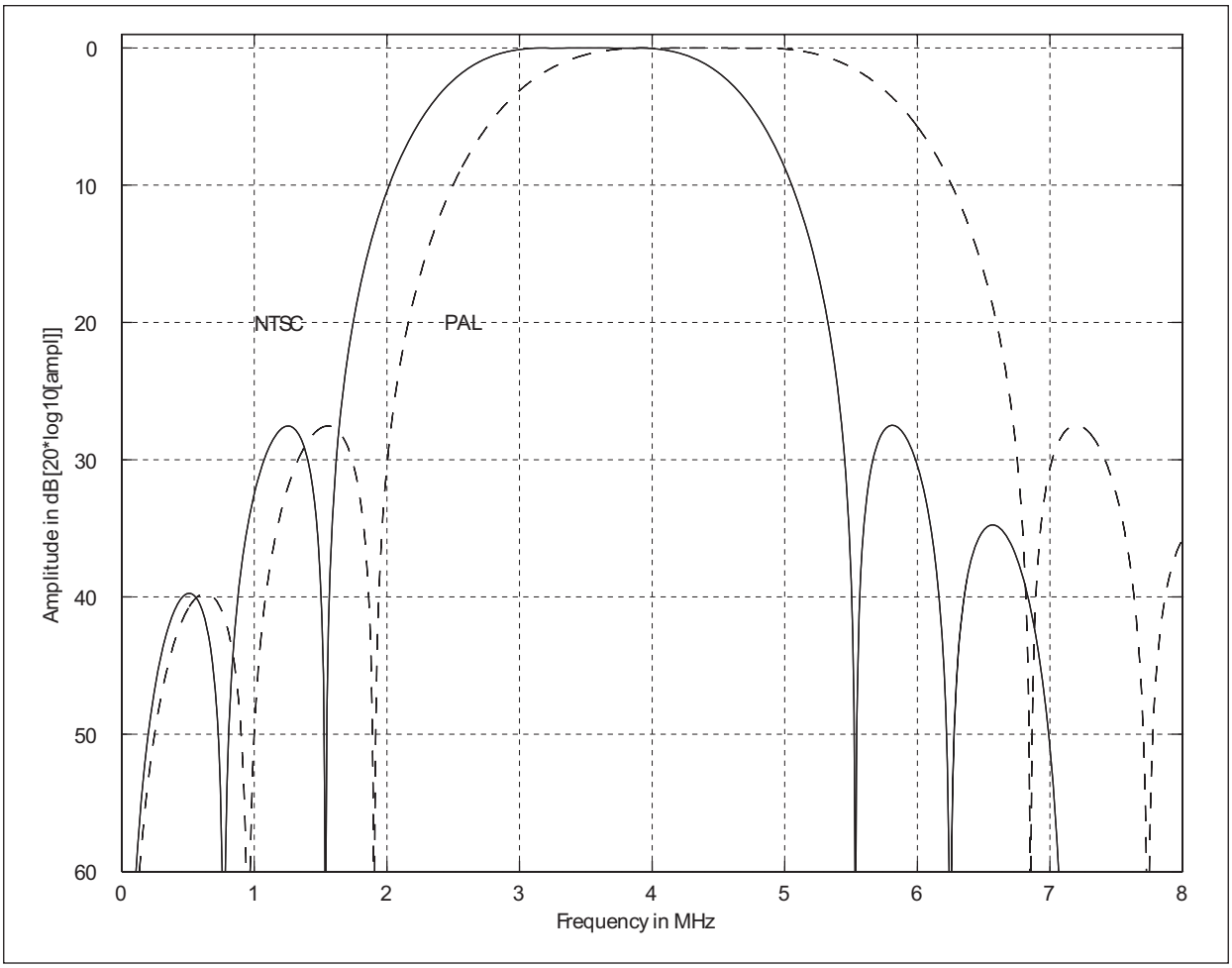
The luma notch filter response for NTSC and PAL video using 13.5-MHz decoding (Y comb filter disabled) is illustrated in Figure 42.

Figure 42. Luma Notch Filter Frequency Responses for NTSC and PAL @ 13.5-MHz Decoding Frequency



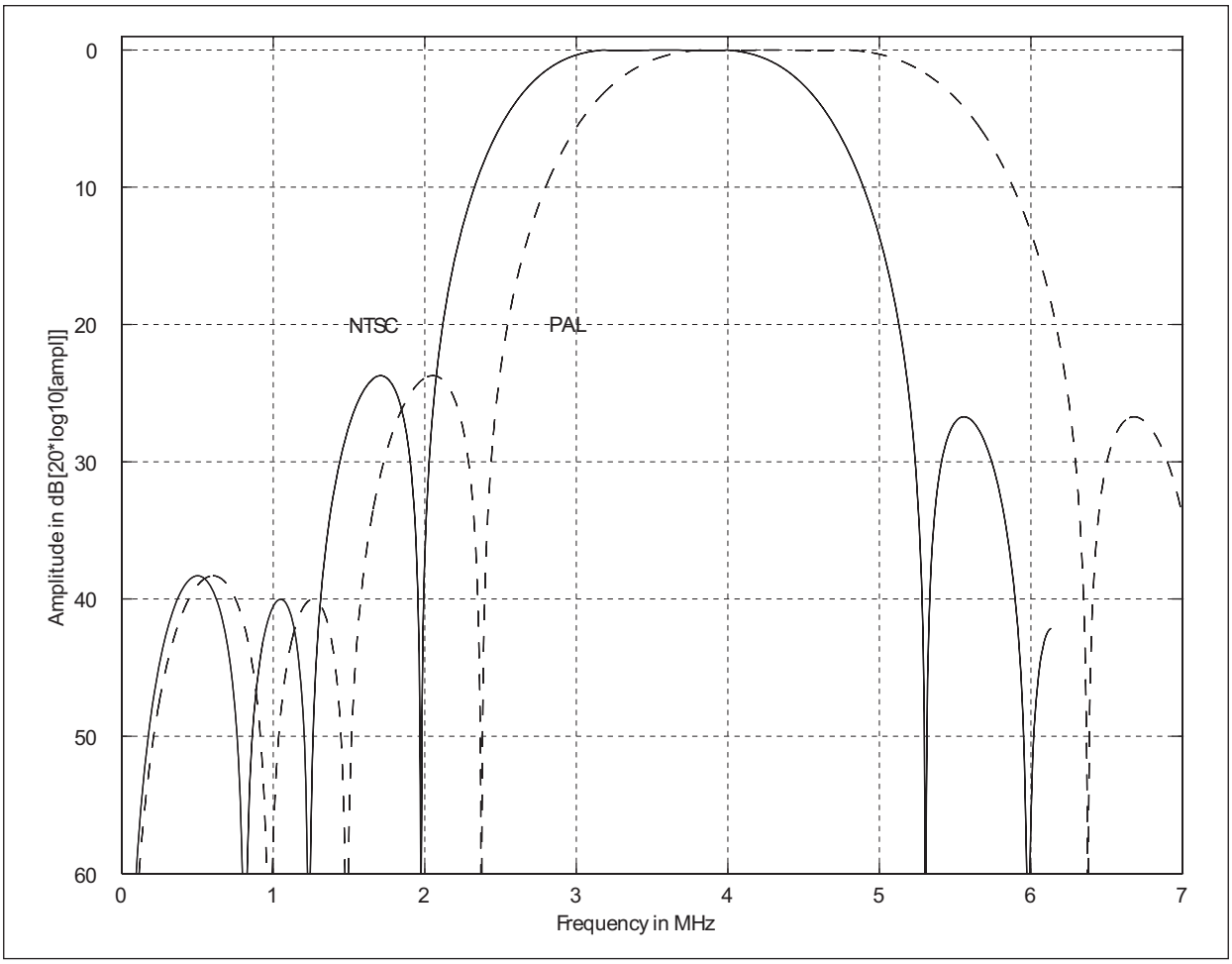
The chroma band-pass filter response for NTSC and PAL video using 4x Fsc decoding is illustrated in Figure 43.

Figure 43. Chroma Band Pass Filter Frequency Responses for NTSC and PAL @ 4x Fsc Decoding Frequencies



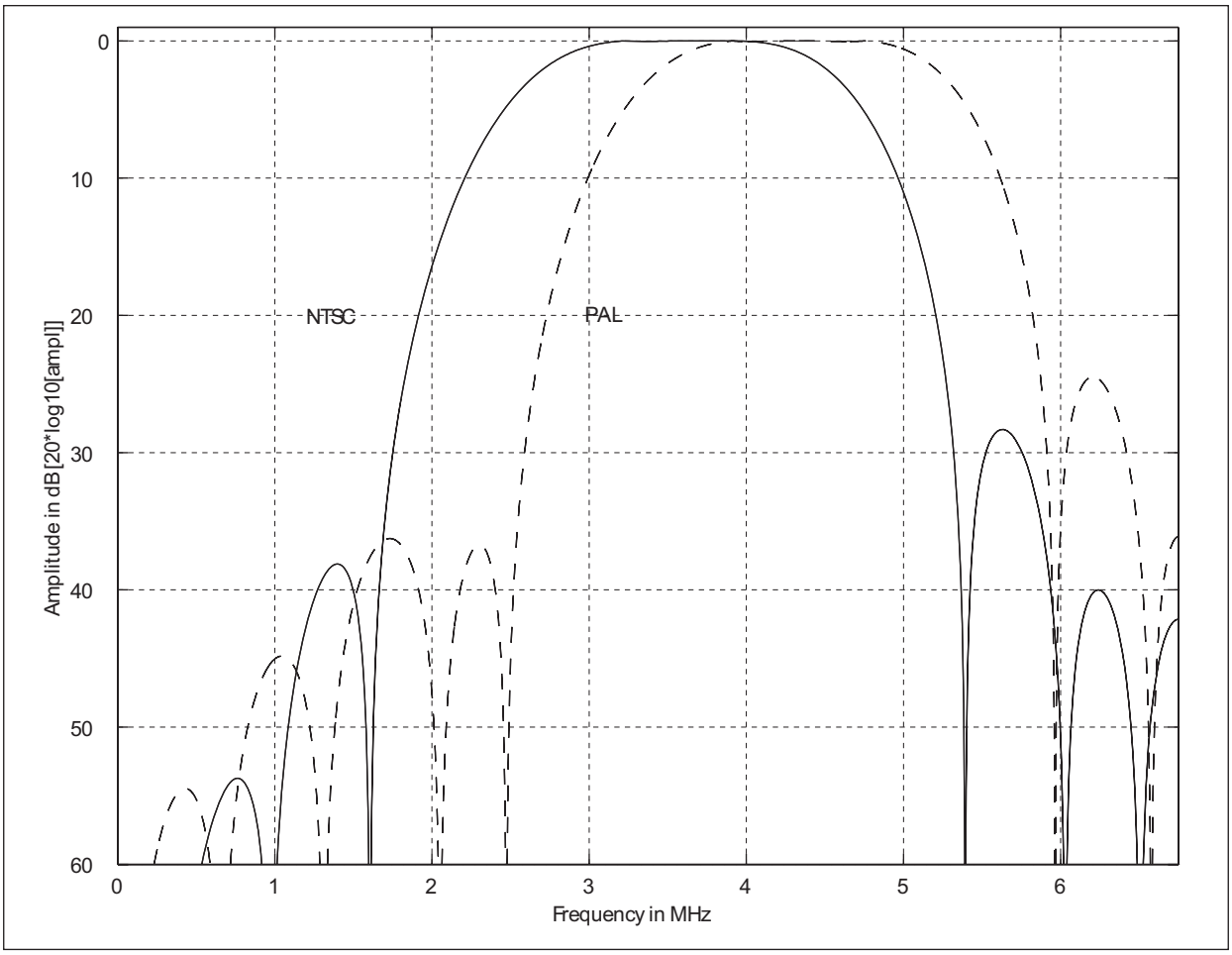
The chroma band-pass filter response for NTSC and PAL video using square pixel decoding is illustrated in Figure 44.

Figure 44. Chroma Band Pass Filter Frequency Responses for NTSC and PAL @ Square Pixel Decoding Frequencies



The chroma band-pass filter response for NTSC and PAL using 13.5-MHz decoding is illustrated in Figure 45.

Figure 45. Chroma Band Pass Filter Frequency Responses for NTSC and PAL @ 13.5-MHz Decoding Frequency



When the adaptive comb filter determines that luma comb decoding is required, the luminance data that is combed out of the chroma data by the band-pass/chroma-comb filter is added back to the notched luma response, thereby restoring the full horizontal luminance content and ensuring a flat frequency response in the luma channel.

When using the video decoder with composite video sources, it is important not to disable the luma notch filter (bit 13 of even and odd field registers Horizontal/Vertical Filters Control). In addition, it is important to ensure that the comb filter bits (bits 5 and 6 of register Horizontal/Vertical Filters Control) remains at the default of 00 when capture sizes of 640x480 through 768x576 are required. For capture sizes below 640x480, the comb filter bits should be set to chroma-comb only (01) because the reduced luminance information is typically below the subcarrier frequency, thus rendering luma comb decoding irrelevant. In this case, bit 27 of the Output Format and 2D Comb Control register (24'h310164) must be disabled by writing a logical 0.

Horizontal/Vertical Filters Control Register

Register 24’h31015C—Even Field

Register 24’h310160—Odd Field

Bits	Type	Default	Name	Description
[13]	RW	1’b0	LNOTCH	0 = Enable notch filter 1 = Disable (recommended for monochrome input—enables full luma bandwidth)
[6:5]	RW	2’b00	COMB	Selects comb filter. 00 = Full Comb 01 = Chroma comb only 10 = Reserved 11 = None

The Output Format and 2H Comb Control register (24’h310164) has additional bit fields related to comb filtering with the defaults configured for optimal quality for the majority of applications. These defaults should not require user intervention unless adaptive comb filtering is required to be switched off, such as when decoding at small capture sizes. However, for PAL video sources, if full luma and chroma Y/C separation is required at resolutions greater than 640x480, bit 26 (PAL_INV_PHASE) must be asserted and a logical 1 written.

Output Format and 2H Comb Control Register

Register 24’h310164

Bits	Type	Default	Name	Description
[31:29]	RO	3’h0		Reserved
[28]	RW	1’b1	PREVREMOD	Enable previous line remodulation; must be used in conjunction with COMBALT = 1
[27]	RW	1’b1	COMBALT	3 Line/2 Line adaptive comb filter 0 = Disable 1 = Enable
[26]	RW	1’b0	PAL_INV_PHASE	Used in PAL 2D comb filter mode.

2.6.8 Video Scaling, Cropping, and Temporal Decimation

The CX25800 provides three mechanisms to reduce the amount of video pixel data in its output stream: downscaling, cropping, and temporal decimation. All three can be controlled independently.

2.6.8.1 Down-Scaling

Horizontal and Vertical Scaling

The CX25800 provides independent and arbitrary horizontal and vertical downscaling. The maximum scaling ratio is 16:1 in both X and Y dimensions. The maximum vertical scaling ratio is reduced from 16:1 when using frames to 8:1 when using fields. The different methods used for scaling luminance and chrominance are described in the following sections.

Field Aligned Vertical Scaling

If Common Interchange Format (CIF) resolution video is viewed at 60/50 Hz rates, the video fields must be field-aligned for proper overlay (sequenced on top of each other successively). This could be done in interlaced Vertical Scaling mode (INT set) which group delays (filters) only one field by one line. The two fields are vertically aligned for overlay, but the two fields have different frequency responses. One has not been filtered, while the other has been line-averaged. An option exists to filter both fields in a similar manner yet maintain proper field alignment. This mode is selected by setting the FDALIGN bit of the Horizontal/Vertical Filters Control to a 1 and setting the VINT bit to a 0 for noninterlaced vertical scaling.

Luminance Scaling— Horizontal Scaling

The first stage in horizontal luminance scaling is an optional pre-filter which provides the capability to reduce anti-aliasing artifacts. It is generally desirable to limit the bandwidth of the luminance spectrum prior to performing horizontal scaling because the scaling of high-frequency components may create image artifacts in the resized image. The optional low-pass filters illustrated in Figures 46 and 47 reduce the horizontal high-frequency spectrum in the luminance signal. Combined luma notch 2x oversampling and optional low-pass filter responses are illustrated in Figures 48 and 49.

The CX25800 implements horizontal scaling through poly-phase interpolation. The CX25800 uses 64 different phases to accurately interpolate the value of a pixel. This provides an effective pixel jitter of less than 4 ns.

In simple pixel- and line-dropping algorithms, noninteger scaling ratios introduce a step function in the video signal that effectively introduces high-frequency spectral components. Poly-phase interpolation accurately interpolates to the correct pixel and line position providing more accurate information. This results in aesthetically pleasing video as well as higher compression ratios in bandwidth-limited applications.

Figure 46. Optional Horizontal Luma Low-Pass Filter Responses for NTSC

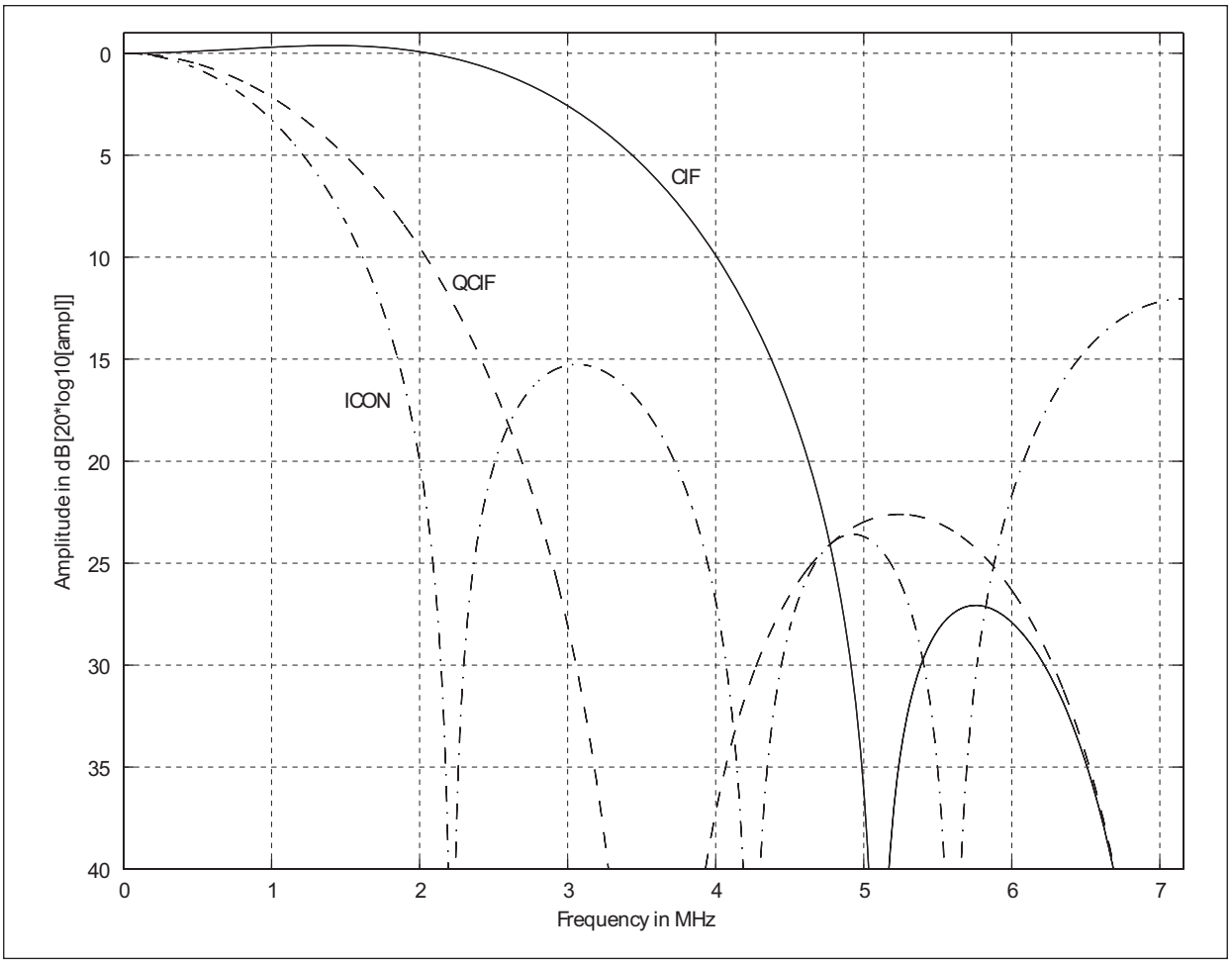


Figure 47. Optional Horizontal Luma Low-Pass Filter Responses for PAL

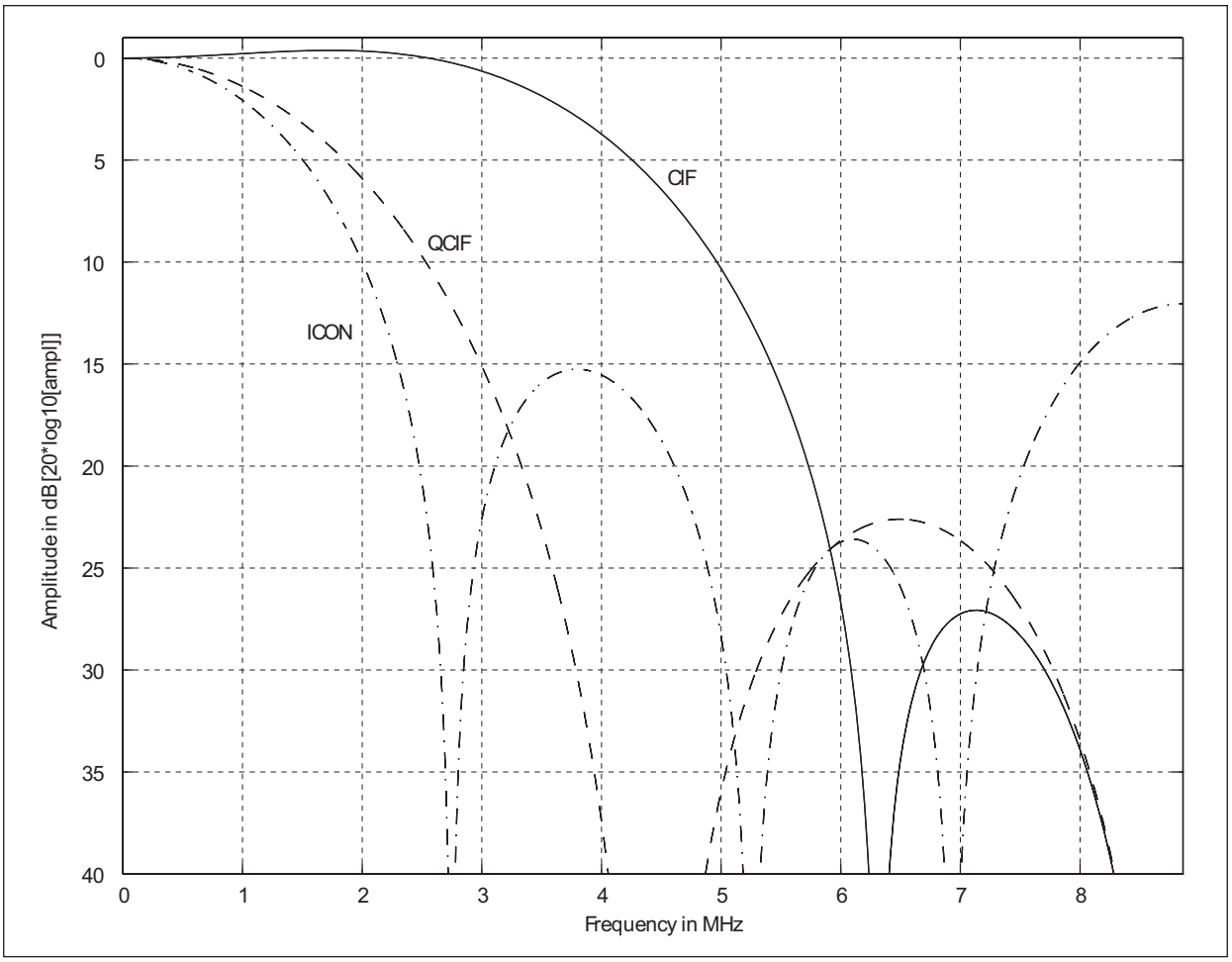


Figure 48. Combined Luma Notch 2x Oversampling and Optional Low-Pass Filter Response for NTSC

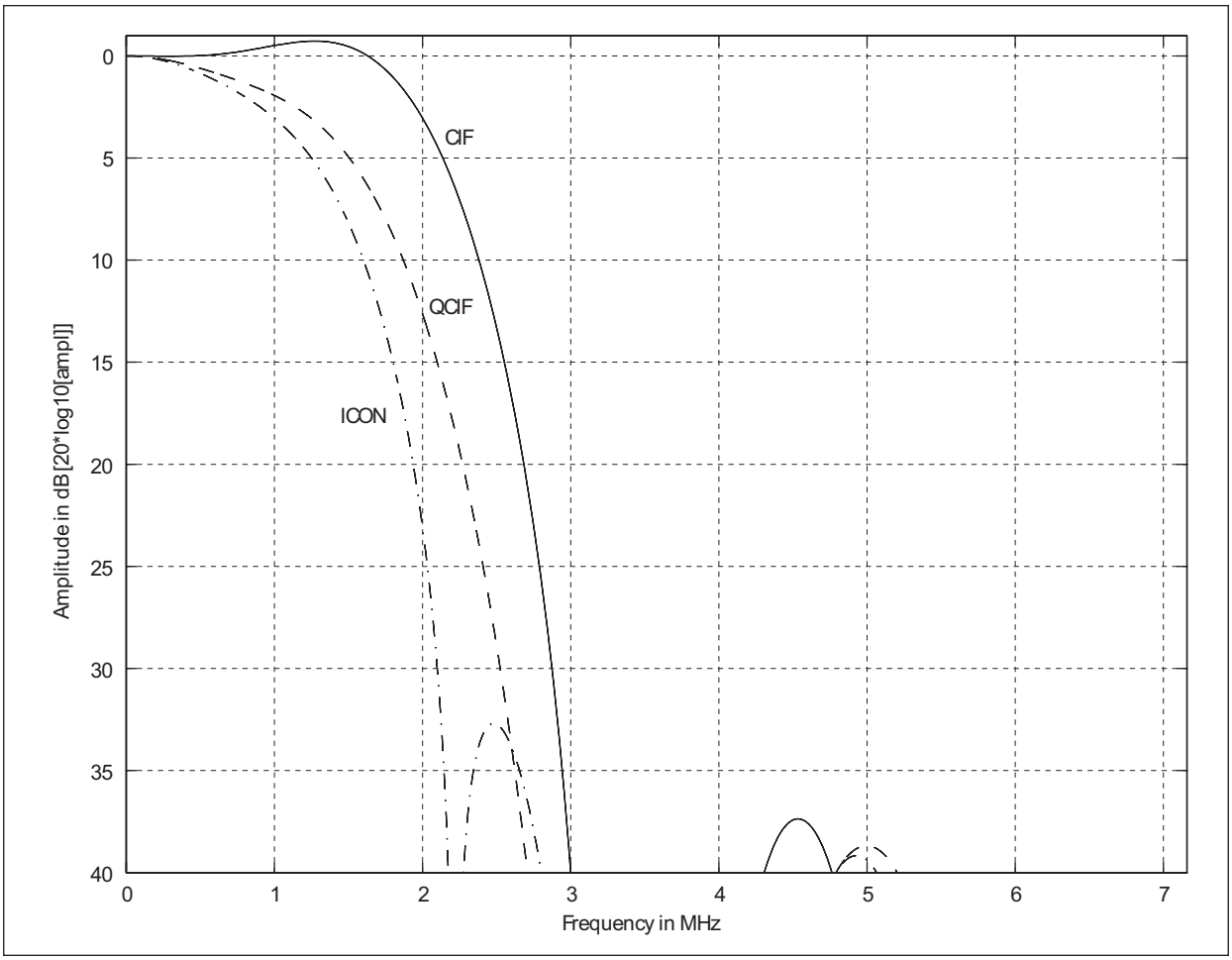
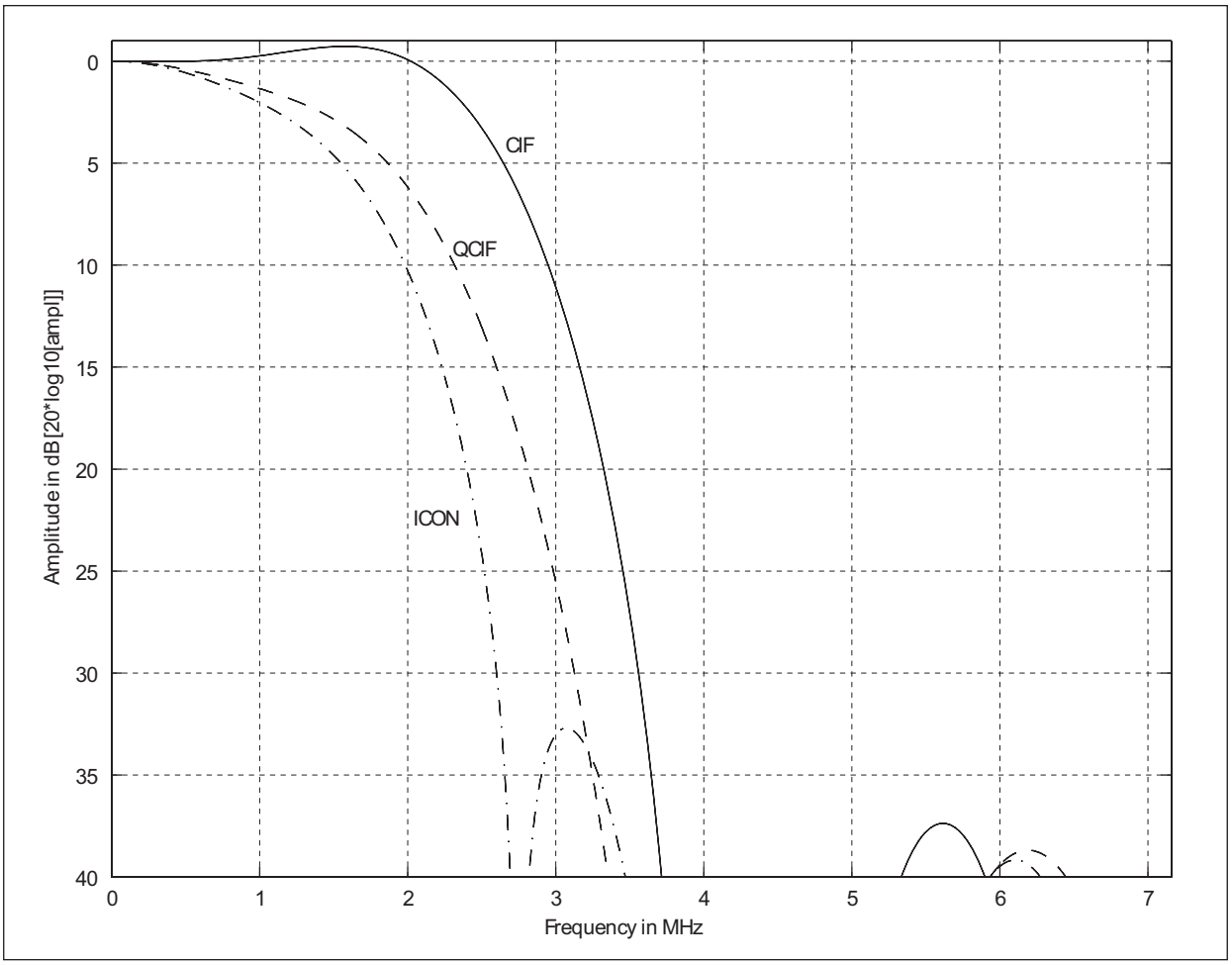


Figure 49. Combined Luma Notch 2x Oversampling and Optional Low-Pass Filter Response for PAL/SECA

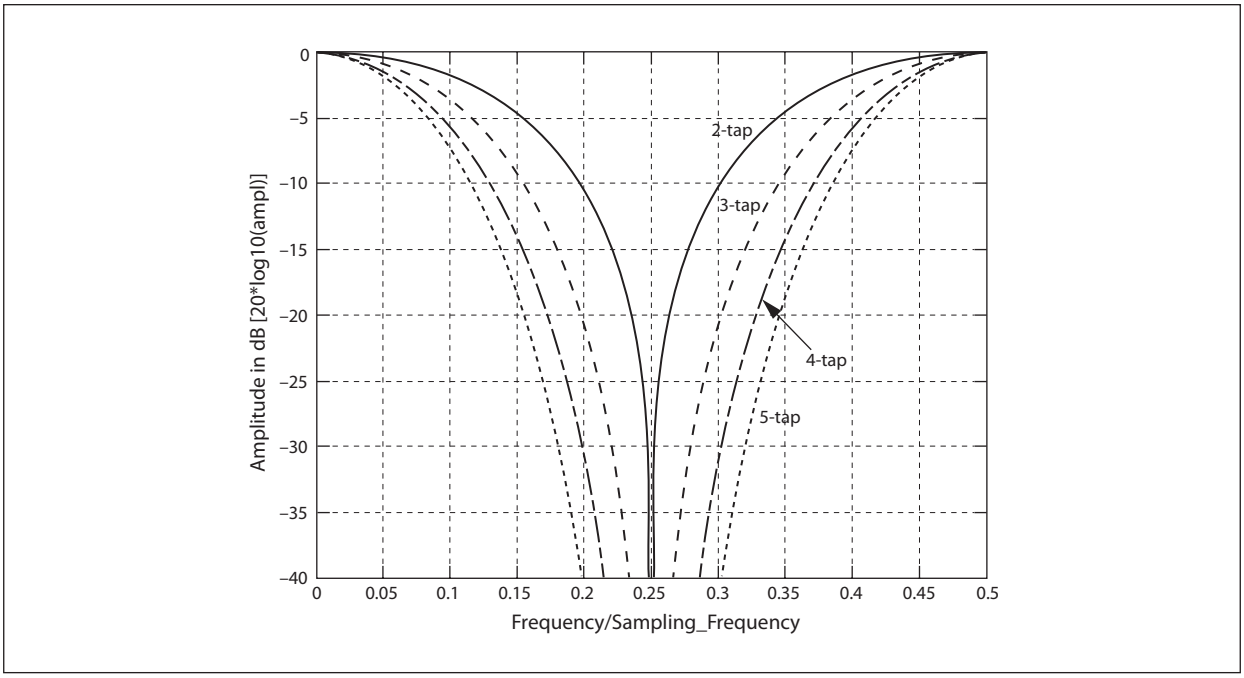


2.6.8.2 Vertical Scaling

For vertical scaling, the CX25800 uses a line store to implement four different filtering options. The filter characteristics are illustrated in Figure 50. The CX25800 provides up to 5-tap filtering to ensure removal of aliasing artifacts.

Bits [2:0] (VFILT) of the Horizontal/Vertical Filters Control register set the number of taps in the vertical filter. The user can select 2, 3, 4, or 5 taps. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure the required data does not overflow the internal FIFO.

Figure 50. Frequency Responses for the Four Optional Vertical Luma Low-Pass Filters



As the scaling ratio increased, the number of taps available for vertical scaling increases. In addition to low-pass filtering, vertical interpolation is also employed to minimize artifacts when scaling to noninteger scaling ratios. In the VFILT section of the Horizontal/Vertical Filters Control register it is also possible to select the multitap filters without interpolation for scaling to integer scaling ratios.

2.6.8.3 Chrominance Scaling

A 4-tap, 64-phase interpolation filter is used for horizontal scaling of chrominance. Vertical scaling of chrominance is implemented by a 2 to 5-tap filter, depending on the size of the image to be scaled. Both Cr and Cb data have their own filter.

2.6.8.4 Video Peaking Filters

The CX25800 enables four different user-selectable peaking filters by programming bits [8:7] (PSEL) of the Horizontal/Vertical Filters Control register. Peaking ranges of +2.0 dB, +3.5 dB, 5.0 dB and +6.0 dB at the NTSC or PAL chroma subcarrier frequencies are offered. These filter responses are illustrated in Figures 51 and 52.

Figure 51. NTSC Peaking Filters

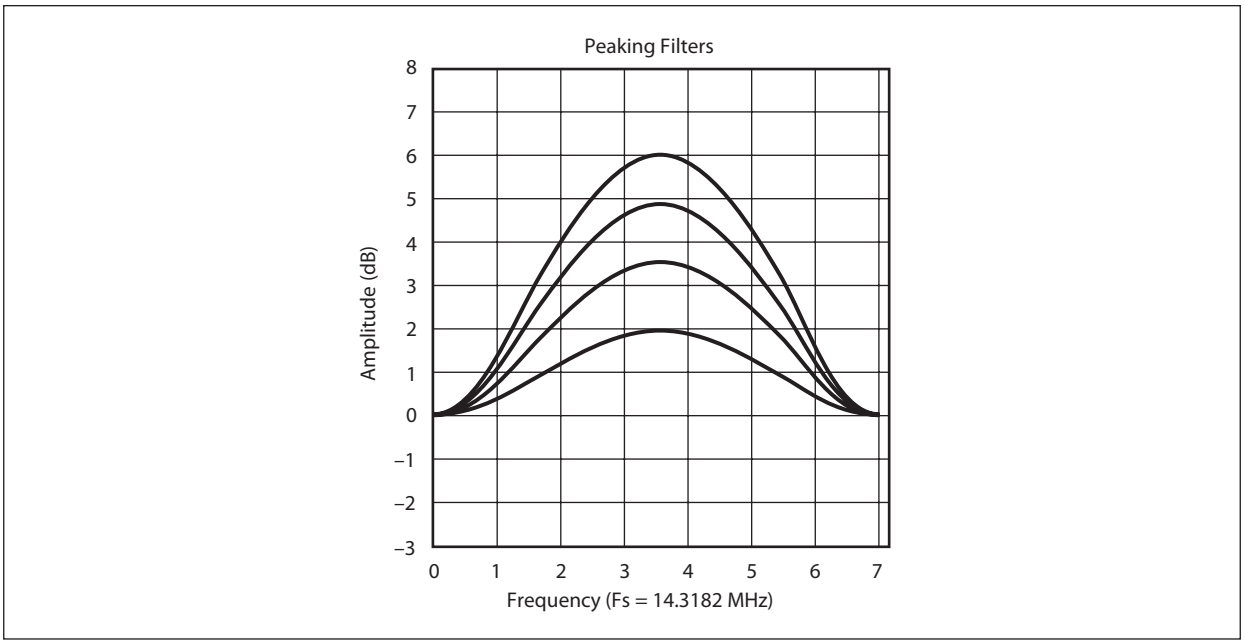
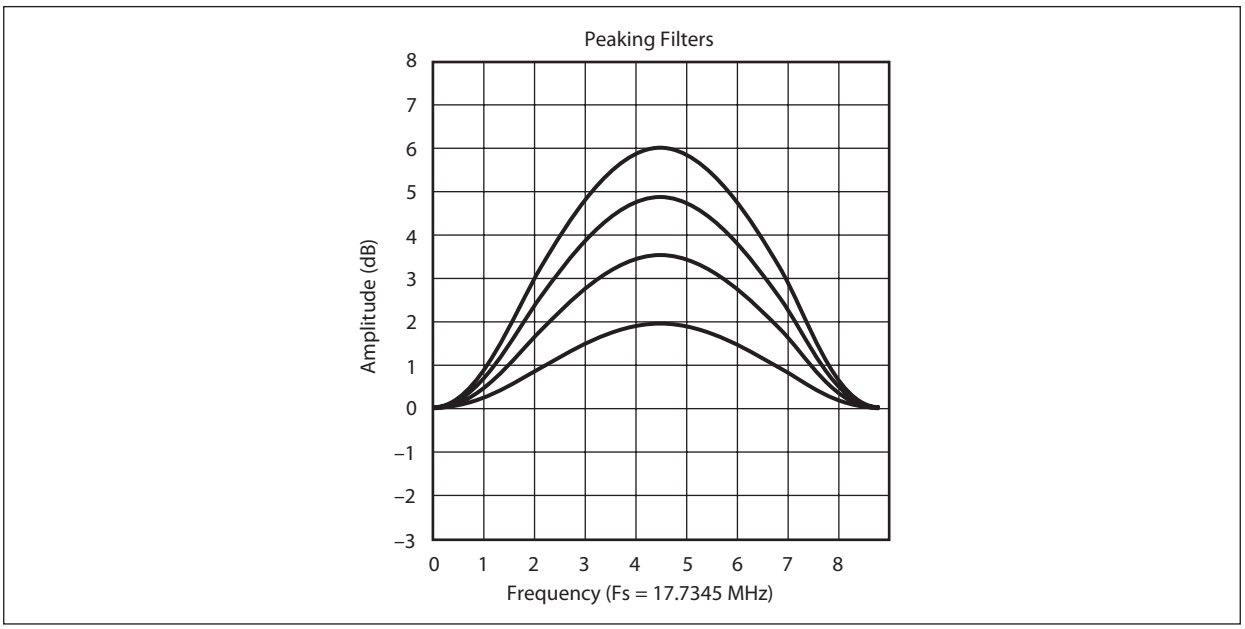


Figure 52. PAL Peaking Filters



2.6.8.5 The Horizontal Scaling Ratio (HSCALE) Register

The 16-bit HSCALE register is programmed with the horizontal scaling ratio. When outputting unscaled video (in NTSC), the CX25800 produces 910 pixels per line. This corresponds to the pixel rate at 4x Fsc. This register is the control for scaling the video to the desired size. For example, square pixel NTSC requires 780 total samples per line, while CCIR601/656 requires 858 total samples per line. The method below uses pixel ratios to determine the scaling ratio. The following formula should be used to determine the scaling ratio to be entered into the 16-bit register:

NTSC HSCALE = $[(910 / P_{Desired}) - 1] \times 4,096$

PAL HSCALE = $[(1,135 / P_{Desired}) - 1] \times 4,096$

where $P_{Desired}$ = Desired number of pixels per line of video, including active, sync, and blanking

For example, to scale PAL input to square-pixel Quarter Common Intermediate Format (QCIF), the total number of horizontal pixels desired is 236:

HSCALE = $[(1,135 / 236) - 1] \times 4,096$

= 12,331

= 0 x 3CF2

An alternative method for determining the HSCALE value uses the ratio of the scaled active region to the unscaled active region as follows:

NTSC HSCALE = $[(754 / HACTIVE) - 1] \times 4,096$

PAL HSCALE = $[(922 / HACTIVE) - 1] \times 4,096$

where HACTIVE = Desired number of pixels per line of video, not including sync or blanking.

In this equation, the HACTIVE value cannot be cropped; it represents the total active region of the video line. This equation produces roughly the same results as using the full-line length ratio shown in the first example. However, due to truncation, the HSCALE values determined using the active pixel ratio method are slightly different from those obtained using the total line length pixel ratio method.

2.6.8.6 The Vertical Scaling Ratio Register (VSCALE)

The 13-bit VSCALE register is programmed with the vertical scaling ratio. It defines the number of vertical lines output by the CX25800. The following formula should be used to determine the value to be entered into this 13-bit register.

VSCALE = (0x10000 – ([(vertical_scaling_ratio) - 1] x 512)) + 0x1FFF)

NOTE: The desired vertical scaling ratio and other inner terms of this equation are decimal and must be converted to hexadecimal to complete the calculation. Worked examples are shown below:

- To vertically scale captured NTSC/PAL to CIF vertical resolution:

VSCALE = (0x10000 – ([(2_2) - 1_1] x 512)) & 0x1FFF

= 0x1E00

- To vertically scale captured NTSC/PAL to QCIF vertical resolution:

VSCALE = (0x10000 – ([(4) - 1] x 512)) & 0x1FFF

= 0x1A00

- To vertically scale captured NTSC/PAL to ICON vertical resolution:

VSCALE = (10000_{16} – ([(8) - 1] x 512)) & 1FFF

= 0x1200

NOTE: When scaling below CIF resolution, it may be useful to use a single field as opposed to using both fields. Using a single field ensures there are no interfield motion artifacts on the scaled output. When performing single field scaling, the vertical scaling ratio is twice as large as when scaling with both fields. For example, CIF scaling from one field does not require any vertical scaling, but when scaling from both fields, the scaling ratio is 50%. Also, the noninterlaced bit should be reset when scaling from a single field (INT = 0 in the VSCALE_HI register).

Table 18 lists scaling ratios for various video formats and the register values required.

Table 18. Scaling Ratios for Popular Formats Using Frequency Values

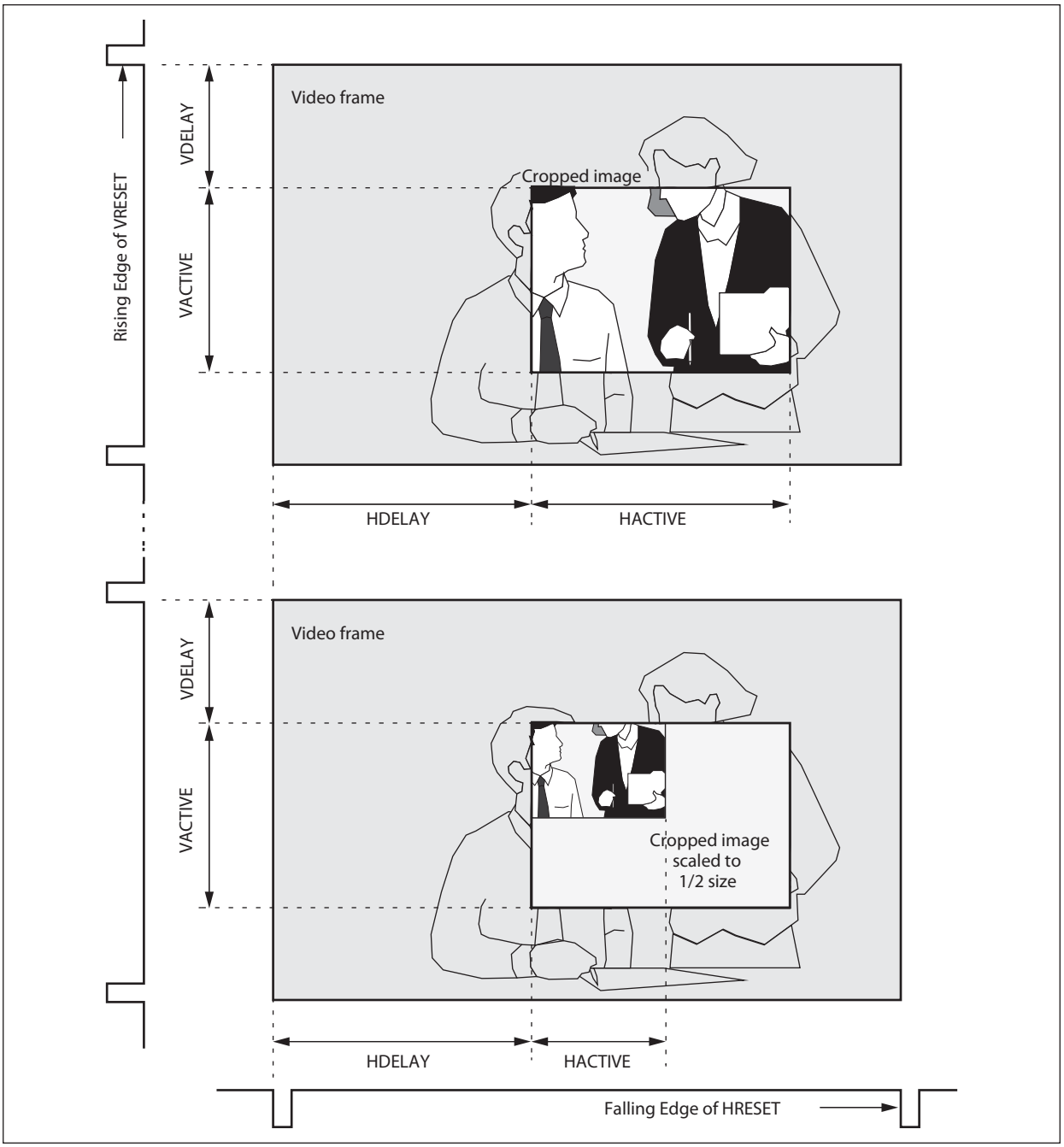
Scaling Ratio	Format	Total Resolution(1)	Output Resolution (Active Pixels)	HSCALE Register Values (HEX)	VSCALE Register Values (HEX)	
					Use Both Fields	Single Field
Full Resolution 1:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	780 × 525 858 × 525 864 × 625 944 × 625	640 × 480 720 × 480 720 × 576 768 × 576	02AA 00F8 0504 033C	0000 0000 0000 0000	N/A N/A N/A N/A
CIF 2:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	390 × 262 429 × 262 432 × 312 472 × 312	320 × 240 360 × 240 360 × 288 384 × 288	1555 11F0 1A09 1679	1E00 1E00 1E00 1E00	0000 0000 0000 0000
QCIF 4:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	195 × 131 214 × 131 216 × 156 236 × 156	160 × 120 180 × 120 180 × 144 192 × 144	3AAA 3409 4412 3CF2	1A00 1A00 1A00 1A00	1E00 1E00 1E00 1E00
ICON 8:1	NTSC SQ Pixel NTSC CCIR601 PAL CCIR601 PAL SQ Pixel	97 × 65 107 × 65 108 × 78 118 × 78	80 × 60 90 × 60 90 × 72 96 × 72	861A 7813 9825 89E5	1200 1200 1200 1200	1A00 1A00 1A00 1A00

FOOTNOTES:
(1) Including sync and the blanking interval.

2.6.9 Image Cropping

Cropping enables the user to output any subsection of the video image. The start of the active area in the vertical direction is referenced to VRESET (the beginning of a new field). In the horizontal direction, it is referenced to HRESET (the beginning of a new line). The dimensions of the active video region are defined by HDELAY, HACTIVE, VDELAY, and VACTIVE. All four registers have 10-bit ranges. The vertical and horizontal delay values determine the position of the cropped image within a frame while the horizontal and vertical active values set the pixel dimensions of the cropped image as illustrated in Figures 53.

Figure 53. Effect of the Delay and Active Registers



2.6.10 Cropping Registers

2.6.10.1 Horizontal Delay Register (HDELAY)

For video decoding, HDELAY is programmed with the number of pixels between horizontal sync and the first pixel of each line to be displayed or captured. HDELAY should be an even number to get Cb as the first pixel, an odd number to get Cr.

The register value is programmed with respect to the scaled frequency clock.

2.6.10.2 Horizontal Active Register (HACTIVE)

For video decoding, HACTIVE is programmed with the actual number of displayed or captured pixels per line.

The register value is programmed with respect to the scaled frequency clock. The video line can be considered a combination of the following three components:

1. Back Porch and Sync: defined by HDELAY
2. Active Video: defined by HACTIVE
3. Front Porch: total scaled pixels—HDELAY through HACTIVE

For uncropped images, the square pixel values for these components at 4 × Fsc are displayed in Table 19.

Table 19. 4x Fsc Pixel Values

Video Standard	CLK × 1 Front Porch	CLK × 1 HDELAY	CLK × 1 HACTIVE	CLK × 1 Total
NTSC	21	135	754	910
PAL	27	186	922	1,135

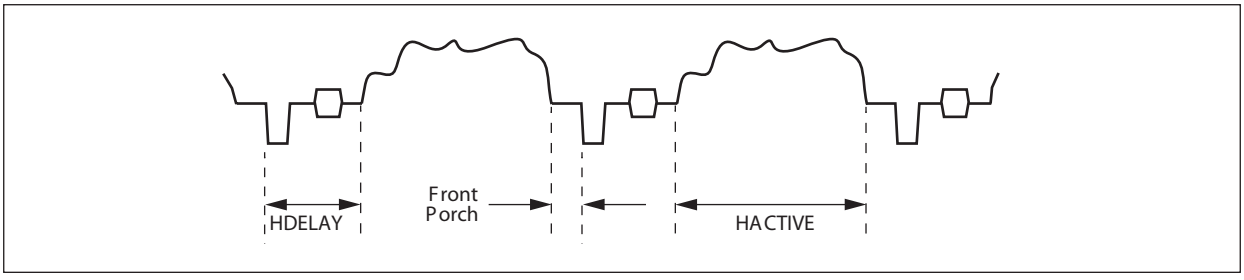
Therefore, for uncropped images the values are:

$$\text{HDELAY (NTSC)} = (135 / 754 \times \text{HACTIVE}) \,\&\, 0 \times 3\text{FE}$$

$$\text{HDELAY(PAL)} = (186 / 922 \times \text{HACTIVE}) \,\&\, 0 \times 3\text{FE}$$

For cropped images, HDELAY can be increased and HACTIVE decreased so that HDELAY + HACTIVE ≤ 889 × HSCALE for NTSC and ≤ 1,108 × HSCALE for PAL. If HDELAY + HACTIVE is too large, then front or back porch pixels, are observed. Regions of the video signal are illustrated in Figure 54.

Figure 54. Regions of the Video Signal



2.6.10.3 The Vertical Delay Register (VDELAY)

For video decoding, VDELAY is programmed with the number of half lines between the end of the serration pulses and the first line to be displayed or captured.

The register value is programmed with respect to the unscaled input signal. VDELAY must be programmed to an even number to avoid apparent field reversal.

2.6.10.4 The Vertical Active Register (VACTIVE)

It is important to note the difference between the implementation of the horizontal (HSCALE, HDELAY, and HACTIVE) and vertical registers (VSCALE, VDELAY, and VACTIVE). Horizontally, HDELAY and HACTIVE are programmed with respect to the scaled pixels defined by HSCALE. Vertically, VDELAY and VACTIVE are programmed with respect to the number of lines before scaling (before VSCALE is applied).

2.6.11 Temporal Decimation

Temporal decimation provides a solution for video synchronization during periods when the full frame rate cannot be supported due to bandwidth and system restrictions.

For example, when capturing live video for storage, system limitations such as hard disk transfer rates or system bus bandwidth may limit the frame capture rate. If these restrictions limit the frame rate to 15 frames per second, the CX25800's time scaling operation enables the system to capture every other frame instead of allowing hard disk timing restrictions to dictate which frame to capture. This maintains an even distribution of captured frames and alleviates the jerky effect caused by systems that burst-in data when the bandwidth becomes available.

The CX25800 provides temporal decimation on either a field or frame basis. Bits [5:0] (TEMPDEC) of the Temporal Decimation register are loaded with a value from 1–60 (NTSC) or 1–50 (PAL). This value is the number of fields or frames skipped by the chip during a sequence of 60 for NTSC or 50 for PAL. Skipped fields and frames are considered inactive, which is indicated by the Active pin remaining low.

Examples:

TDEC	= 0×02—	Decimation is performed by frames. Two frames are skipped per 60 frames of video, assuming NTSC decoding. Frames 1–29 are output normally, then Active remains low for 1 frame. Frames 31–59 are then output, followed by another frame of inactive video.
TDEC	= 0×9E —	Decimation is performed by fields. Thirty fields are output per 60 fields of video, assuming NTSC decoding. This value outputs every other field (every odd field) of video starting with field 1 in frame 1.
TDEC	= 0×01—	Decimation is performed by frames. One frame per 50 frames of video is skipped, assuming PAL decoding.
TDEC	= 0×00—	Decimation is not performed. Full-frame rate video is output by the CX25800.

When changing the programming in the Temporal Decimation register, 0×00 should be loaded first and then the decimation value. This ensures that the decimation counter is reset to 0. If 0 is not loaded first, the decimation may start on any field or frame in the

sequence of 60 (or 50 for PAL). On power-up, this preload is not necessary because the counter is internally reset.

When decimating fields, the TDALGN bit in the TDEC register can be programmed to choose whether the decimation starts with an odd or even field. If the TDALGN bit is set to logical 0, the first field dropped during the decimation process is an odd field. Conversely, setting the TDALGN bit to logical 1 causes the even field to be dropped first in the decimation process.

2.6.12 Video Adjustments

The CX25800 provides programmable hue, contrast, saturation, and brightness.

2.6.12.1 The Hue Adjust Register

The Hue Adjust register (HUE) is used to offset the hue of the decoded signal. In NTSC, the hue of the video signal is defined as the phase of the subcarrier with reference to the burst. The value programmed in this register is added to or subtracted from the phase of the subcarrier, which effectively changes the hue of the video. The hue can be shifted by ±90 degrees.

2.6.12.2 The Contrast Adjust Register

The Contrast Adjust register (CONTRAST), also called the luma gain, provides the ability to change the contrast from approximately 0–200 percent of the original value. The decoded luma value is multiplied by the 8-bit coefficient loaded into this register.

2.6.12.3 The Saturation Adjust Registers

The Saturation Adjust registers (VSAT, USAT) are additional color adjustment registers. It is a multiplicative gain of the U and V signals. The values programmed in these registers are the coefficients for the multiplication. The saturation range is from approximately 0–200 percent of the original value, over an 8-bit range.

2.6.12.4 The Brightness Register

The Brightness register (BRIGHT) is simply an offset for the decoded luma value. The programmed value is added to or subtracted from the original luma value, which changes the brightness of the video output. The luma output is in the range of 0–255. Brightness adjustment can be made over a range of –128 to +127 (2s complement).

2.6.12.5 Automatic Chrominance Gain Control (ACGC)

The ACGC compensates for reduced chrominance and color-burst amplitudes. Here, the color-burst amplitude is calculated and compared to nominal. The color-difference signals are then increased or decreased in amplitude according to the color-burst amplitude difference from nominal. The range of chrominance gain is 0.5–2 times the original amplitude. This compensation coefficient is then multiplied by the saturation adjust value for a total chrominance gain range of 0–2 times the original signal. ACGC may be disabled.

2.6.13 Low Color Detection and Removal

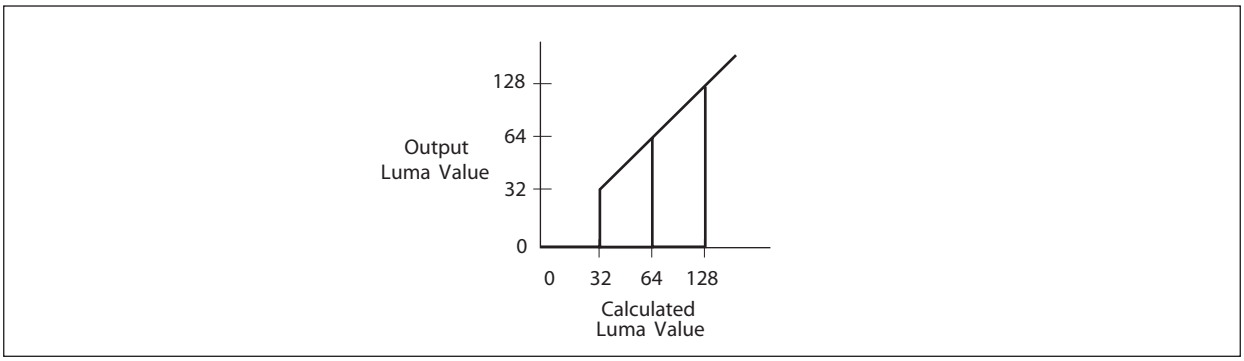
If a color-burst of 25 (NTSC) or 35 (PAL) percent or less of the nominal amplitude is detected for 127 consecutive scan lines, the color-difference signals U and V are set to 0. When the low color detection is active, the reduced chrominance signal is still separated from the composite signal to generate the luminance portion of the signal. The resulting Cr and Cb values are 128. Output of the chrominance signal is re-enabled when a color-burst of 43 (NTSC) or 60 (PAL) percent or greater of nominal amplitude is detected for 127 consecutive scan lines. Low color detection and removal may be disabled.

2.6.14 Coring

The CX25800 video decoder can perform a coring function in which it forces all values below a programmed level to 0. This is useful because the human eye is more sensitive to variations in black images. By taking near-black images and turning them into black, the image appears clearer to the eye.

Four coring values can be selected: 0, 32, 64, or 128 above black. If the total luminance level is below the selected limit, the luminance signal is truncated to the black value. If the luma range is limited (i.e., black is 16), the coring circuitry automatically takes this into account and references the appropriate value for black. Coring is illustrated in Figure 55.

Figure 55. Coring Map



2.6.15 VBI Data Output Interface

A video frame is composed of 525 lines for NSTC and 625 for PAL. Figure 56 illustrates an NTSC video frame in which there are a number of distinct regions. The video image or picture data is contained in the odd and even fields within lines 21–263 and 283–525, respectively. Each field of video also contains a region for vertical synchronization (lines 1–9 and 264–272) and a region which can contain nonvideo ancillary data (lines 10–20 and 273–283). These regions between the vertical synchronization region and the video picture region are referred to as the VBI portion of the video signal. Figure 57 illustrates a PAL video frame.

Figure 56. Regions of the NTSC Video Frame

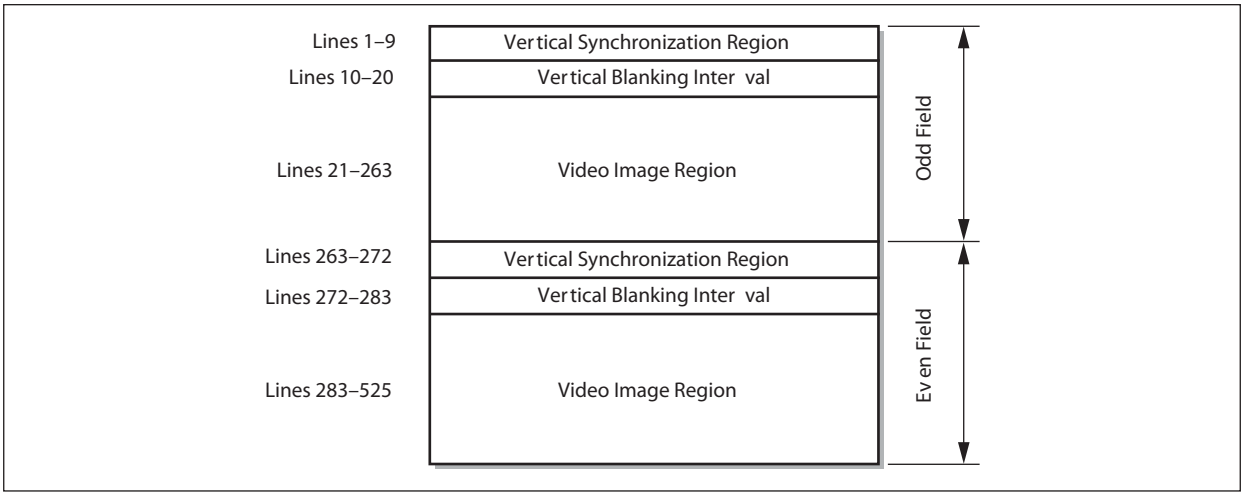
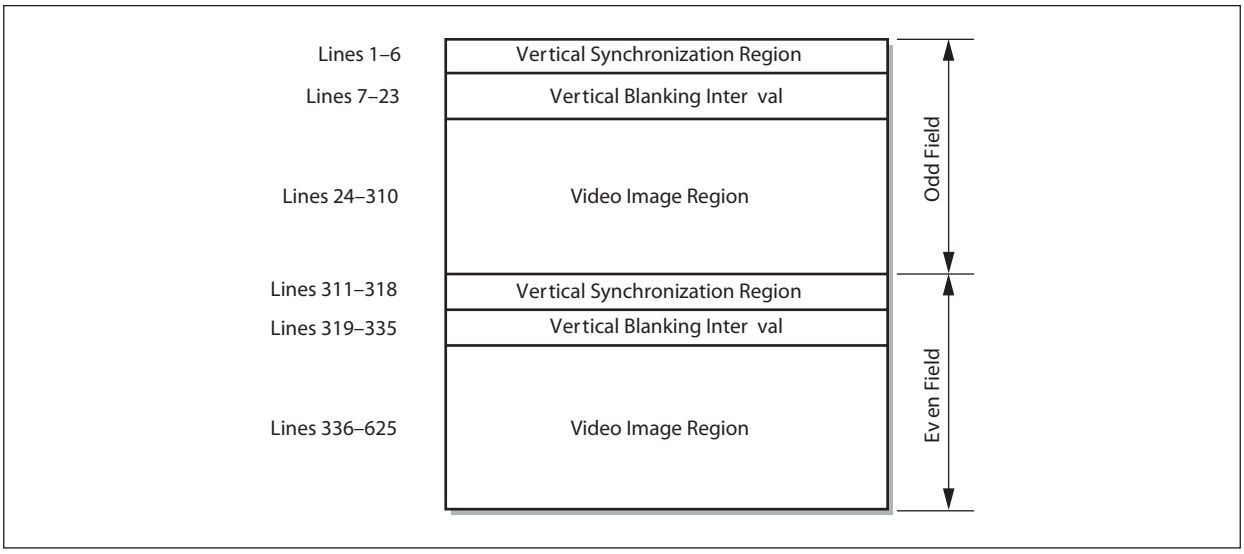


Figure 57. Regions of the PAL Video Frame (Fields 1, 2, 5, and 6)



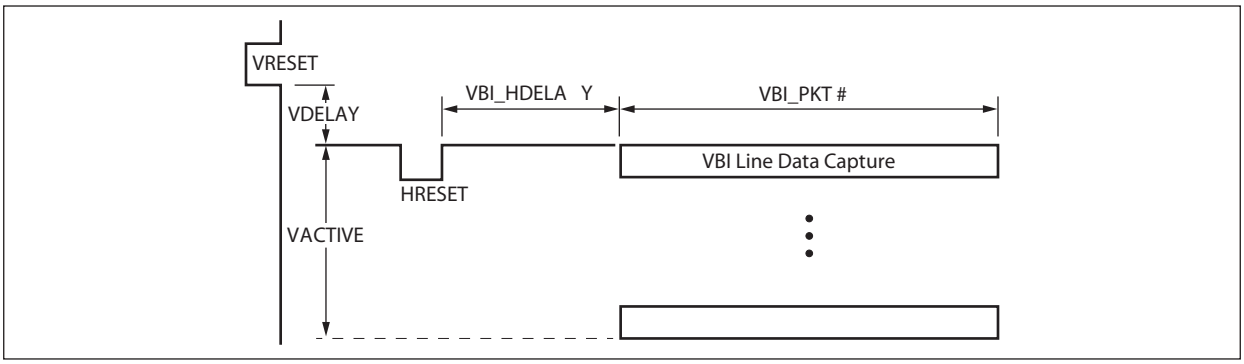
The CX25800 is able to capture VBI data and store it in the host memory for subsequent processing by the VBI decoder software. Two modes of VBI capture exist, VBI line output mode and VBI frame output mode. Both types of data can be captured during the same field.

2.6.16 VBI Line Output Mode

In the VBI Line Output mode, VBI capture occurs during the vertical blanking interval. The start of VBI data capture is set by the VBI_HDELAY bit in the VBI Packet Size/ Delay register, and is in reference to the trailing edge of the HRESET signal. The number of dwords of VBI data is selected by the user. Each dword contains 4 VBI bytes, and each VBI pixel consists of 2 VBI samples. For example, for a given 800 pixel line in the VBI region, there exist 1,600 VBI samples, which are equivalent to 400 dwords of VBI data. The VBI_PKT_HI and VBI_PKT_LO register bits are concatenated to create the 9-bit value for the number of dwords to be captured.

VBI line data capture occurs when the CAPTURE_VBI_EVEN register bit is enabled for the even field and the CAPTURE_VBI_ODD register bit is enabled for the odd field. The VBI data is sampled at a rate of 8 × Fsc and is stored in the FIFO as a sequence of 8-bit samples. Line mode VBI data starts horizontally beginning at the VBI_HDELAY pixels from the trailing edge of HRESET and ending after the VBI_PKT number of dwords. Line mode VBI data starts vertically beginning at the first line following VRESET and ending at VACTIVE. VBI register settings can be changed only on a per-frame basis. The VBI timing is illustrated in Figure 58.

Figure 58. VBI Timing



Once the VBI data has been captured and stored in the CX25800 FIFO, it is treated as any other type of data. It is output over the PCI bus through RISC instructions. If the number of VBI lines desired by the user is smaller than the entire vertical blanking region, the extra data is discarded by the use of the SKIP RISC instruction. Alternatively, if the user desires a larger VBI region in the VBI line output mode, the vertical blanking region can be extended by setting the VDELAY register to the appropriate value. The VBI line output mode can, in effect, extend the VBI region to the entire field.

In the VBI frame output mode, VBI data capture occurs in the active video region and includes all the horizontal blank/sync information in the data stream. This feature can be used to provide a high-quality still-capture of video. The data is vertically bound beginning at the first line during VACTIVE and ending after a fixed number of packets. The data stream is packetized into a series of 256-dword blocks.

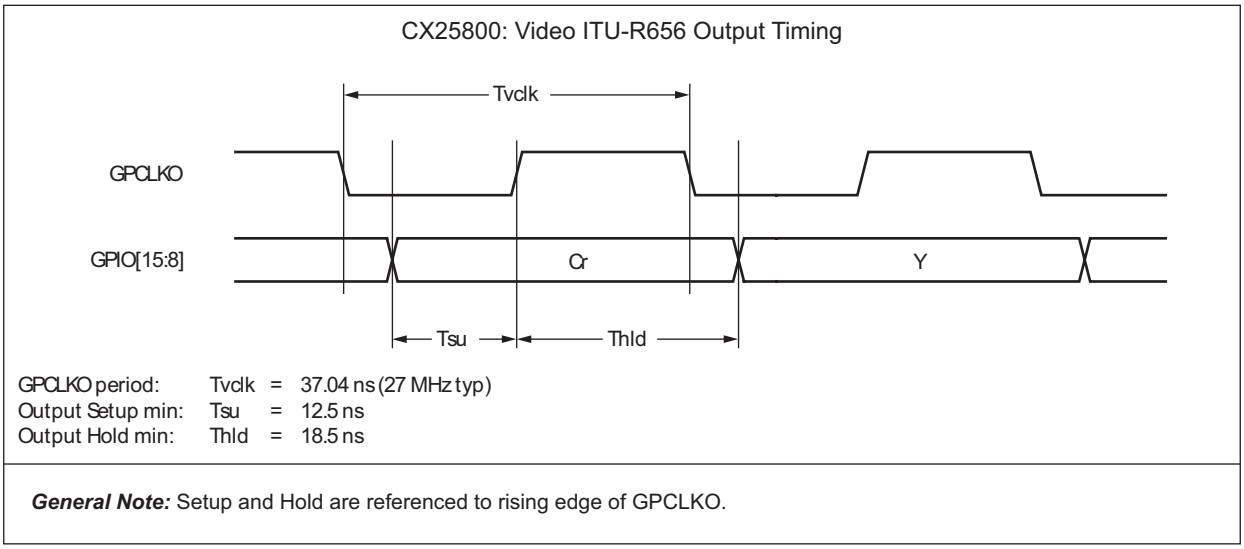
A fixed number of dword blocks (434 for NTSC and 650 for PAL) are captured during each field. This is equivalent to 111,104 dwords for NTSC (434 × 256 dwords) and 166,400 dwords for PAL (650 × 256 dwords) per field. The VBI frame capture region can be extended to include the 10 lines prior to the default VACTIVE region by setting the EXT_FRAME register bit. VDELAY must also be set to its minimum value of 2. The extended dword block size is 450 dword blocks for NTSC and 674 dword blocks for PAL.

The VBI frame data capture occurs during the even field when the CAPTURE_EVEN register bit is set and the COLOR_EVEN bit is set to raw mode, and during the odd field when the CAPTURE_ODD register bit is set and the COLOR_ODD bit is set to raw mode. The captured data stream is continuous and not aligned with HSYNC.

2.6.17 ITU-R656 Output Interface

This port outputs 4:2:2, 720 × 480 interlaced YCrCb pixels with embedded timing codes synchronous with a 27-MHz output clock (see Figure 59). Refer to Section 2.3 for details on configuring the GPIO pins to enable this mode.

Figure 59. Video ITU-R 656 Output Timing



General Note: Setup and Hold are referenced to rising edge of GPCLKO.

2.6.18 ITU-R656/VIP 2.0 8-bit Pixel Input Interface

This port accepts 720 × 480 interlaced 4:2:2 YCrCb pixels synchronous with a 27-MHz input clock. Bit 17 of the Input Format register toggles between the analog video input and the digital pixel ITU-R656/VIP data input.

Input Format Register

Register 24'h310104

Bits	Type	Default	Name	Description
[17]	RW	1'b0	PESRC_SEL	0 = pixel engine input selects analog input data and clock 1 = pixel engine input selects digital input data and clock (VIP input source)

Figure 60, MPEG 2 Decoder to CX25800 ITU-R656 Connection, Example 1 and Figure 61, MPEG 2 Decoder to CX25800 ITU-R656 Connection, Example 2 illustrate ITU-R.BT656 timing from an external MPEG II decoder to the CX25800's Pixel Input Interface.

Alternatively, this port can accept 4:2:2 720 × 480 progressive YCrCb pixels synchronous with a 54-MHz input clock.

Refer to Section 2.3 for details on configuring the GPIO pins to enable this mode.

Figure 60. MPEG 2 Decoder to CX25800 ITU-R656 Connection, Example 1

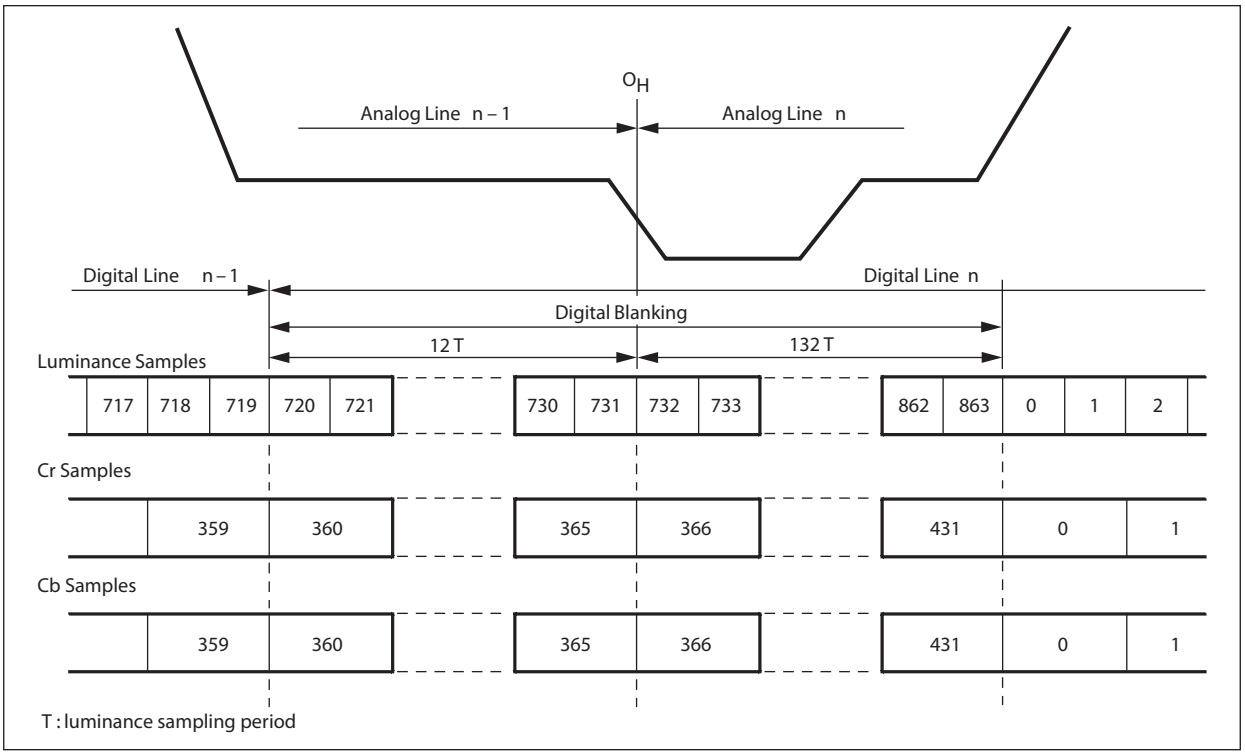
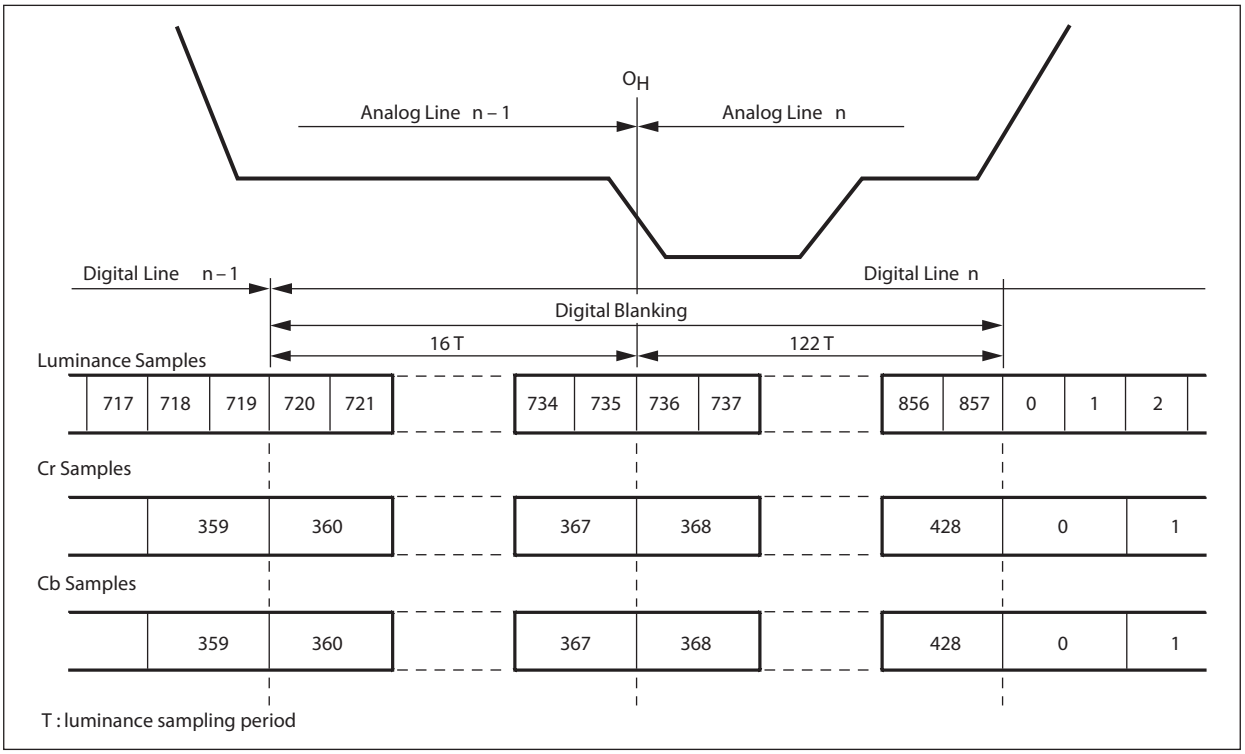


Figure 61. MPEG 2 Decoder to CX25800 ITU-R656 Connection, Example 2



2.7 VIP 2.0 Host Master

2.7.1 Introduction

The VESA VIP 2.0 Host Master interface is a high-bandwidth, minimal-pin-count interface for connecting multiple video components.

Refer to the Video Electronics Standards Association (VESA) Video Interface Port, version 2, specification for full implementation details.

The VIP 2.0 Host Master interface enables the CX25800 to communicate with devices which are compliant with either the VIP 1.1 or 2.0 slave specification.

2.7.2 VIP 2.0 Host Master Overview

The VIP 2.0 Host Master Interface (VHMI) is a slave on the CX25800 Internal Peripheral Bus (IPB). The IPB is designed so that there is only one master, the DMAC, but several slaves—the VHMI being one of them. Data is fetched from the VHMI by the DMAC after a request for service is indicated by the VHMI's assigned DMA request channel.

The VHMI can be configured for either a 2-, 4-, or an 8-bit data path. If only a 2-bit data interface is required, then the 6 remaining unused data path pins can be assigned as GPIO. Table 20 describes the CX25800's 11 VHMI pins.

Table 20. VIP Host Master Interface Pin Description

Pin No	Pin Name	Dir	Type	Signal	VIP 2.0 Host Master Signals Description (5 or 11 Pins)
20	VIPCLK	O	—	VIP Clock	VIP master output clock
8–17	VHAD[7/1:0]	I/O	—	VIP Host Address/Data	This multipurpose bus is used to transfer commands, addresses, and data between the CX25800 and VIP slave devices. This bus is only fully utilized when communicating with a VIP slave that supports the 4x host port. The VIP 2.0 specification declares that all VIP devices must be backward compatible with VIP 1.1 specification. This means that the CX25800 must support those VIP devices that have 2-, 4-, or 8-pin HAD bus implementations.
18	VHCTL	I/O	—	VIP Host Control	The VHCTL pin is a shared control pin that is used to begin, end, or throttle data transfers. Because this is a shared pin, the VIP specification clearly outlines the protocol for driving this signal to avoid conflict.
19	VIRQ#	I/O	od	VIP Interrupt Request	The VIRQ pin is an open-collector interrupt pin that can be used by a VIP slave device to interrupt the CX25800.

The VIP Configuration and VIP Terminate registers below are required to configure and control the VHMI port.

VIP Configuration

24'h340048—VIP_CFG Register

Bits	Type	Default	Name	Description
[11:8]	RW	4'b1111	VIP time-out_length	VIP time-out length
[7:6]	RW	2'b00	Peripheral #1 config	2'b00 = 1x configuration (2-bit) 2'b01 = 2x configuration (4-bit) 2'b10 = reserved 2'b11 = 4x configuration (8-bit)
[5:4]	RW	2'b00	Peripheral #2 config	See channel #1 above.
[3:2]	RW	2'b00	Peripheral #3 config	See channel #1 above.
[1:0]	RW	2'b00	Peripheral #4 config	See channel #1 above.

VIP Terminate

24'h340060—VIP_XFER_TERMINATE Register

Bits	Type	Default	Name	Description
[14:5]	RW	10'h3FF	P1_retry_limit	This caps off how many retries are attempted to a VIP slave on a target read or write.
[4]	WO	1'b1	VIP_soft_rst	Software controllable reset for the entire VIP design. (VIP Clock Domain Only) Writing a 0 causes a reset pulse to the VIP block.
[3]	WO	1'b1	ISI_soft_rst	Software controllable reset for the ISI design core. Writing a 0 causes a reset pulse to the ISI block.
[2]	WO	1'b0	Terminate_ch1	Writing a 1 to this register causes the VIP transfer state machine for the register R/W channel to be reset.
[1]	WO	1'b0	Terminate_ch2	Writing a 1 to this register causes the VIP transfer state machine for the downstream DMA channel to be reset.
[0]	WO	1'b0	Terminate_ch3	Writing a 1 to this register causes the VIP transfer state machine for the upstream DMA channel to be reset.

The following VIP Interrupt registers are listed below: VIP Interrupt Control, VIP Interrupt Mask, VIP Interrupt Status, VIP Interrupt Masked Status, and VIP Interrupt Set Status.

VIP Interrupt Control

24'h34C05C—VIP_INTR_CTRL Register

Bits	Type	Default	Name	Description
[1]	RW	1'b0	VIP_intr_type	Level or Edge sensitive interrupt. 0 = level sensitive 1 = edge sensitive
[0]	RW	1'b0	VIP_intr_polarity	Interrupt polarity. 0 = active low 1 = active high

VIP Interrupt Mask

24'h200080—VIP_INT_MASK Register

Bits	Type	Default	Name	Description
[21:0]	RW	22'b0	VIP_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the VIP_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

VIP Interrupt Status

24'h200084—VIP_INT_STATUS Register

Bits	Type	Default	Name	Description
[21]	RR	1'b0	VIP_TM_OUT	Set when a time-out occurs during a VIP transfer.
[20]	RR	1'b0	VIP_EXT	Set when the VIP external interrupt signal is asserted.
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[13]	RR	1'b0	UP_SYNC	Set when number of lines or bytes do not match the upstream VIP RISC program expectations.
[12]	RR	1'b0	DN_SYNC	Set when number of lines or bytes do not match the downstream VIP RISC program expectations.
[9]	RR	1'b0	UPF_UF	Set when upstream VIP FIFO underflow condition is being handled.
[8]	RR	1'b0	DNF_OF	Set when downstream VIP FIFO overflow condition is being handled.
[5]	RR	1'b0	UP_RISCI2	Set when the IRQ2 bit in a upstream VIP RISC instruction is set.
[4]	RR	1'b0	DN_RISCI2	Set when the IRQ2 bit in a downstream VIP RISC instruction is set.
[1]	RR	1'b0	UP_RISCI1	Set when the IRQ1 bit in a upstream VIP RISC instruction is set.
[0]	RR	1'b0	DN_RISCI1	Set when the IRQ1 bit in a downstream VIP RISC instruction is set.

VIP Interrupt Masked Status

24'h200088—VIP_INT_MSTAT Register

Bits	Type	Default	Name	Description
[21:0]	RO	22'b0	VIP_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

VIP Interrupt Set Status

24'h20008C—VIP_INT_SSTAT Register

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	VIP_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

2.7.3 VIP 2.0 Host Master System Functionality

The VIP Host Master interface is designed to perform the following three main tasks:

1. Stream data from a VIP slave into host memory through the PCI bus (Downstream DMA)
2. Stream data to a VIP slave that is sent over the PCI bus by the host (Upstream DMA)
3. Host access to register space on connected VIP slave devices

All data streaming across the VIP bus should be done through the two DMA channels that have been set up to handle this function. Once the DMAC is set up to point to the correct source or destination in memory, the VIP interface block must be set up to kick off the transfer. The following sections describe the protocol for both downstream and upstream data transfers. The VIP DMA registers are listed in the following paragraphs.

APB DMAC Current Buffer Pointer

24'h3000A0—DMA29_PTR1 Register

24'h3000A4—DMA30_PTR1 Register

Bits	Type	Default	Name	Description
[23:2]	RO	22'hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

APB DMAC Current Table Pointer

24'h3000E0—DMA29_PTR2 Register

24'h3000E4—DMA30_PTR2 Register

Bits	Type	Default	Name	Description
[23:2]	RW*	22'hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

APB DMAC Buffer Limit

24'h300120—DMA29_CNT1 Register

24'h300124—DMA30_CNT1 Register

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

APB DMAC Table Size

24'h300160—DMA29_CNT2 Register

24'h300164—DMA30_CNT2 Register

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.

General Purpose Counter (Immediate Access)

24'h34C020—VIPD_GP_CNT Register

24'h34C024—VIPU_GP_CNT Register

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	{x}_GP_CNT	General purpose counter used by RISC.

General Purpose Counter Control (Immediate Access)

24’h34C030—VIPD_GP_CNT_CNTRL Register

24’h34C034—VIPU_GP_CNT_CNTRL Register

Bits	Type	Default	Name	Description
[1:0]	WO	2’b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

VIP Streaming Enable (Immediate Access)

24’h34C040—VIP_STREAM_EN Register

Bits	Type	Default	Name	Description
[5]	RW	1’b0	VIPU_RISC_EN	RISC Controller enable for the VIP interface upstream DMA channel.
[4]	RW	1’b0	VIPD_RISC_EN	RISC Controller enable for the VIP interface downstream DMA channel
[1]	RW	1’b0	VIPU_FIFO_EN	Enable for pulling data out of the VIP upstream DMA FIFO or CDT.
[0]	RW	1’b0	VIPD_FIFO_EN	Enable for fetching downstream data from the external source.

VIP Upstream DMA Control Register #1

24'h34004C—VIPU_DMA_CTRL1 Register

Bits	Type	Default	Name	Description
[23:0]	RW	24’hxxxxxx	VIPU_DST_ADDR	VIP upstream APB DMA destination address.

VIP Downstream DMA Control Register #2

24'h340050—VIPD_DMA Register

Bits	Type	Default	Name	Description
[23:0]	RW	24’hxxxxxx	VIPD_SRC_ADDR	VIP downstream APB DMA source address.

VIP Downstream DMA Control Register #3

24'h340054—VIPD_DMA Register

Bits	Type	Default	Name	Description
[11:0]	RW	12’hxxx	VIP_LNGTH	VIP downstream transfer count in bytes.

VIP Downstream DMA Control Register #4

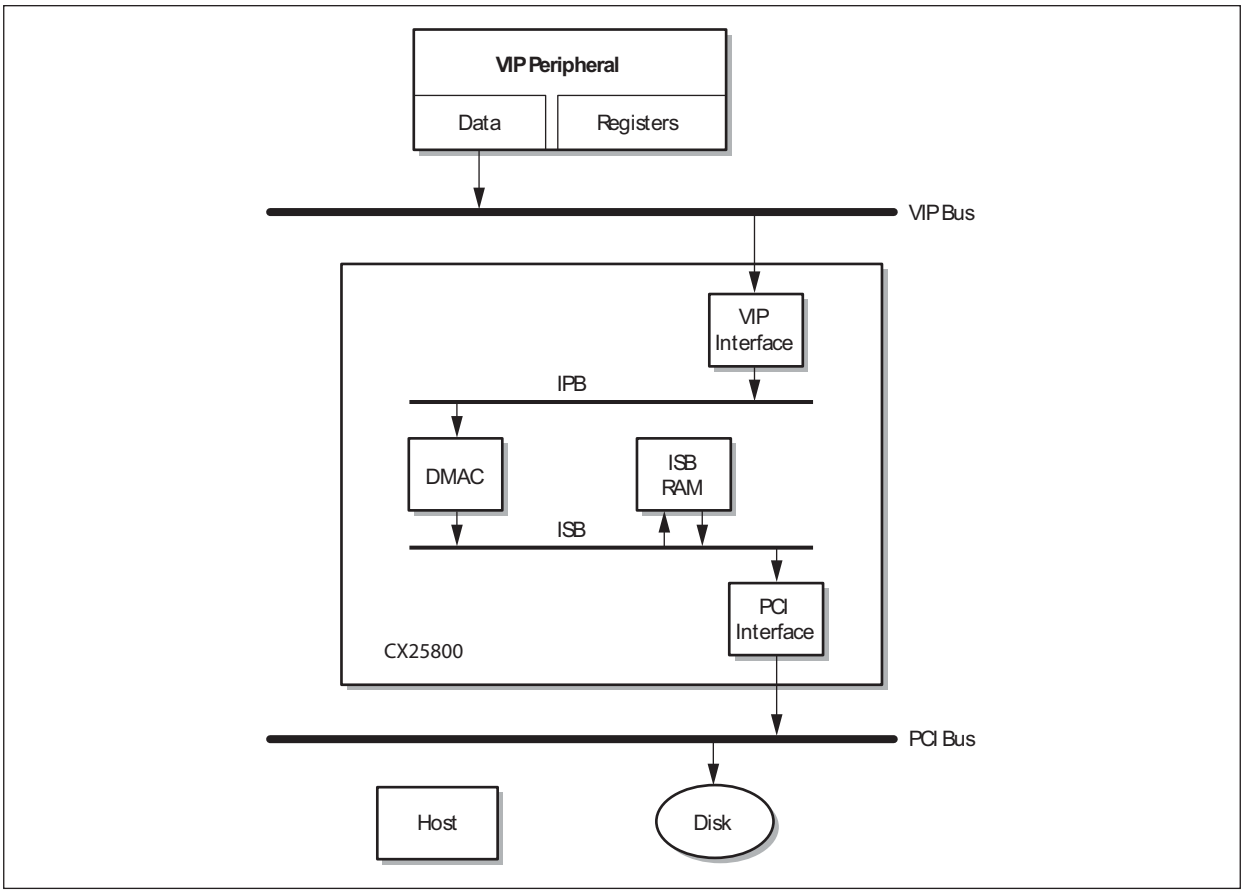
24'h340058—VIP_BURST_LENGTH Register

Bits	Type	Default	Name	Description
[15:8]	RW	8'FF	VIPU_BURST_LNGTH	VIP Maximum Upstream burst length in terms of VIP data cycles. This value entered here should depend upon VIP mode (1x, 2x, 4x) 1x = 1 byte/data cycle, 2x = 2 bytes/data cycle…
[7:0]	RW	8'hFF	VIPD_BURST_LNGTH	Maximum burst length for downstream transfers.

2.7.3.1 Downstream DMA Channel

This is a case the VIP interface module fetches the PSI data from the VIP bus and places it into a small transfer buffer within the VIP interface module. The VHMI then initiates a transfer request to the DMAC. Next, the DMAC moves the data into a temporary buffer within the Internal System Bus (ISB) RAM. The data is then sent over the PCI bus to the host for processing.

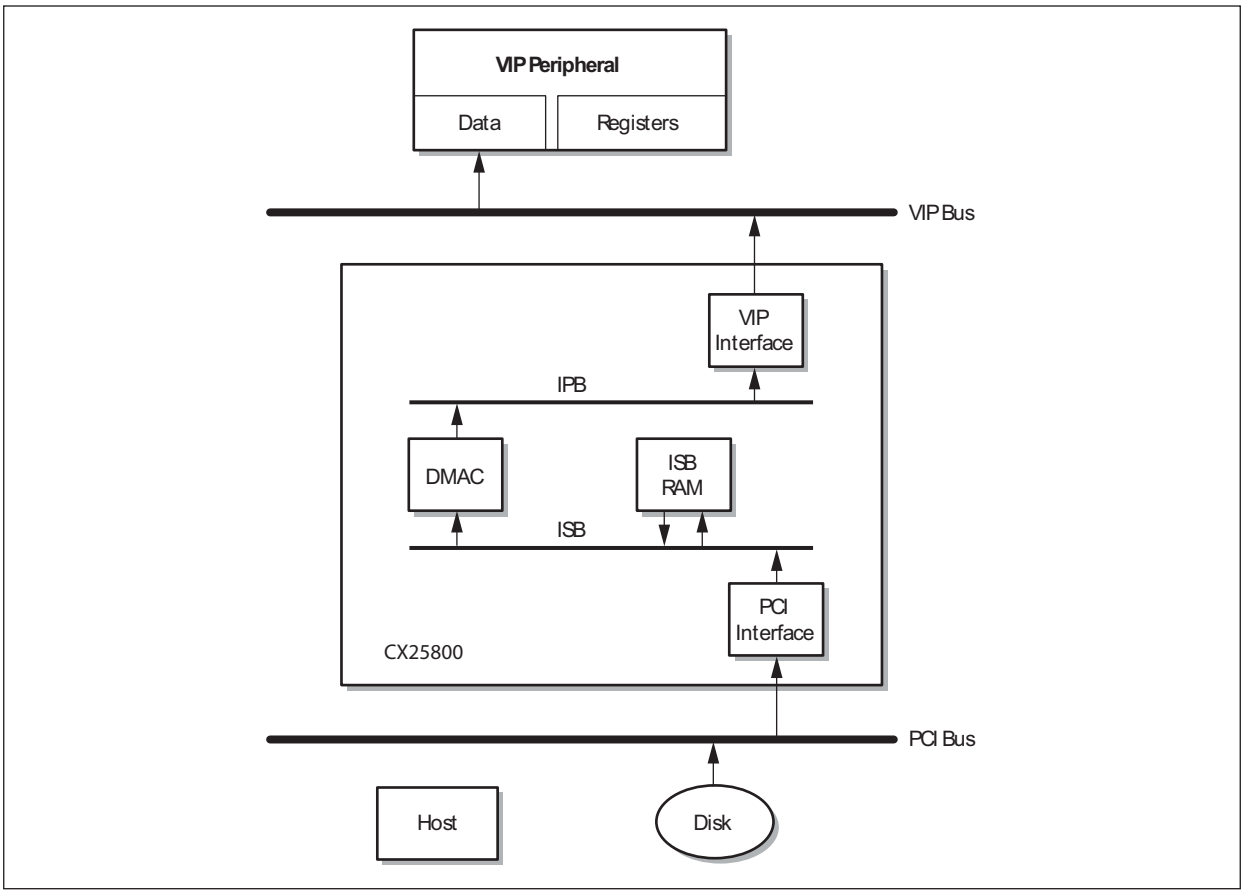
Figure 62. Data Transfer from VIP 2.0 Slave to Host through CX25800



2.7.3.2 Upstream DMA Channel

This is a scenario where the host is sending compressed high-definition video data from the disk to the VIP interface. The host sends the compressed data to the CX25800 through the PCI bus, where the PCI Interface module decodes the PCI data and places it into the ISB RAM. Next, the DMAC and VIP modules are programmed with the appropriate data to set up the transfer of the compressed data from the ISB RAM to the VIP module (see Data Transfer from Host to VIP Slave through). The VIP Interface module then reformats the data and sends it out on the VIP bus to the all-format decoder.

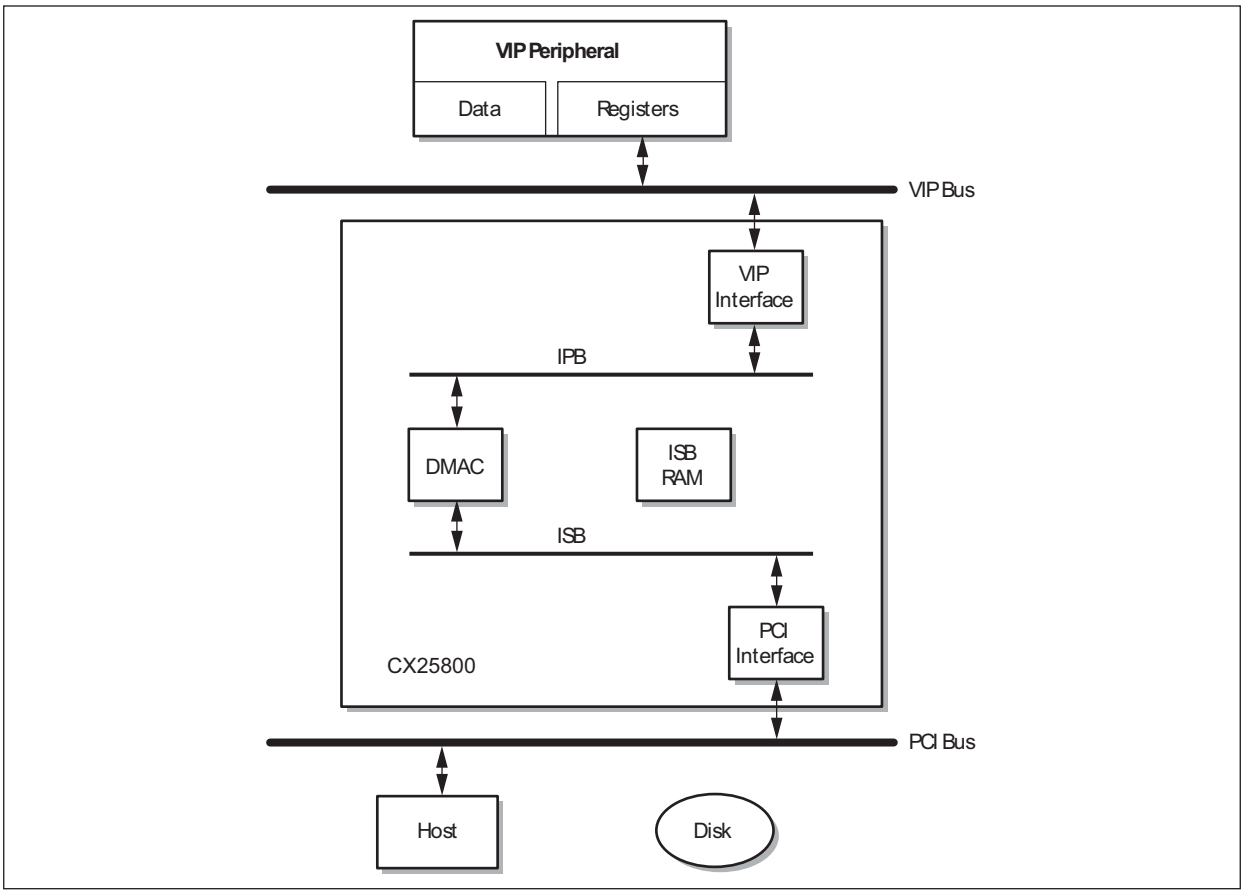
Figure 63. Data Transfer from Host to VIP Slave through CX25800



2.7.3.3 VIP External Register Access

This scenario is one in which the host wants to read or write registers in a device that is attached to the VIP Host Port (see Figure 64).

Figure 64. VIP External Register Access



2.7.3.4 VIP Local Register Access

All internal VIP Host-Master Interface registers are mapped into the IPB address space so they are accessible from any ISB or IPB masters. This allows the host to access this register space through the PCI module.

2.7.4 VIP Memory Space

The VIP register space in the CX25800 has been divided up into the following three main groups:

1. Local VIP registers
2. External status registers
3. Main external peripheral address space

Memory VIP space is defined in Table 2-20.

Table 21. Memory VIP Space

Address Range	Size	Description
340000–3407FF	4,031 Bytes	VIP delayed across local registers
340800–340FBF	—	Reserved
341000–341FFF	4 kB	Peripheral 1 address space
342000–342FFF	4 kB	Peripheral 2 address space
343000–343FFF	4 kB	Peripheral 3 address space
344000–344FFF	4 kB	Peripheral 4 address space
345000–34FFFF	—	Reserved
345FFF–345000	256 bytes	Peripheral 1 predefined FIFO and status ports
346000–346FFF	256 bytes	Peripheral 2 predefined FIFO and status ports
347000–347FFF	256 bytes	Peripheral 3 predefined FIFO and status ports
348000–348FFF		Peripheral 4 predefined FIFO and status ports
345000–34BFFF		Reserved
34C000–34CFFF		VIP Immediate access local registers

2.7.5 VIP Address Space

Through the VIP port, we have access to a maximum of 4 kB of address space for each VIP peripheral and the internal VIP registers. The VHMI supports up to 4 slaves in any given configuration, which means there are 16 kB of CX25800 memory space directly mapped to these external devices. This direct-mapped address space is supplied for external register access and is not intended for streaming data to the peripheral. All data streaming should be through the DMA channels.

3 Electrical Interfaces

3.1 Input Interfaces

3.1.1 Analog Signal Selection

The CX25800 contains an on-chip 4:1 multiplexer (VMUX[4:1]) that can be used to switch between four composite video inputs. An AGC circuit enables the CX25800 to compensate for nonstandard amplitudes in the analog signal input.

3.1.2 Multiplexer Considerations

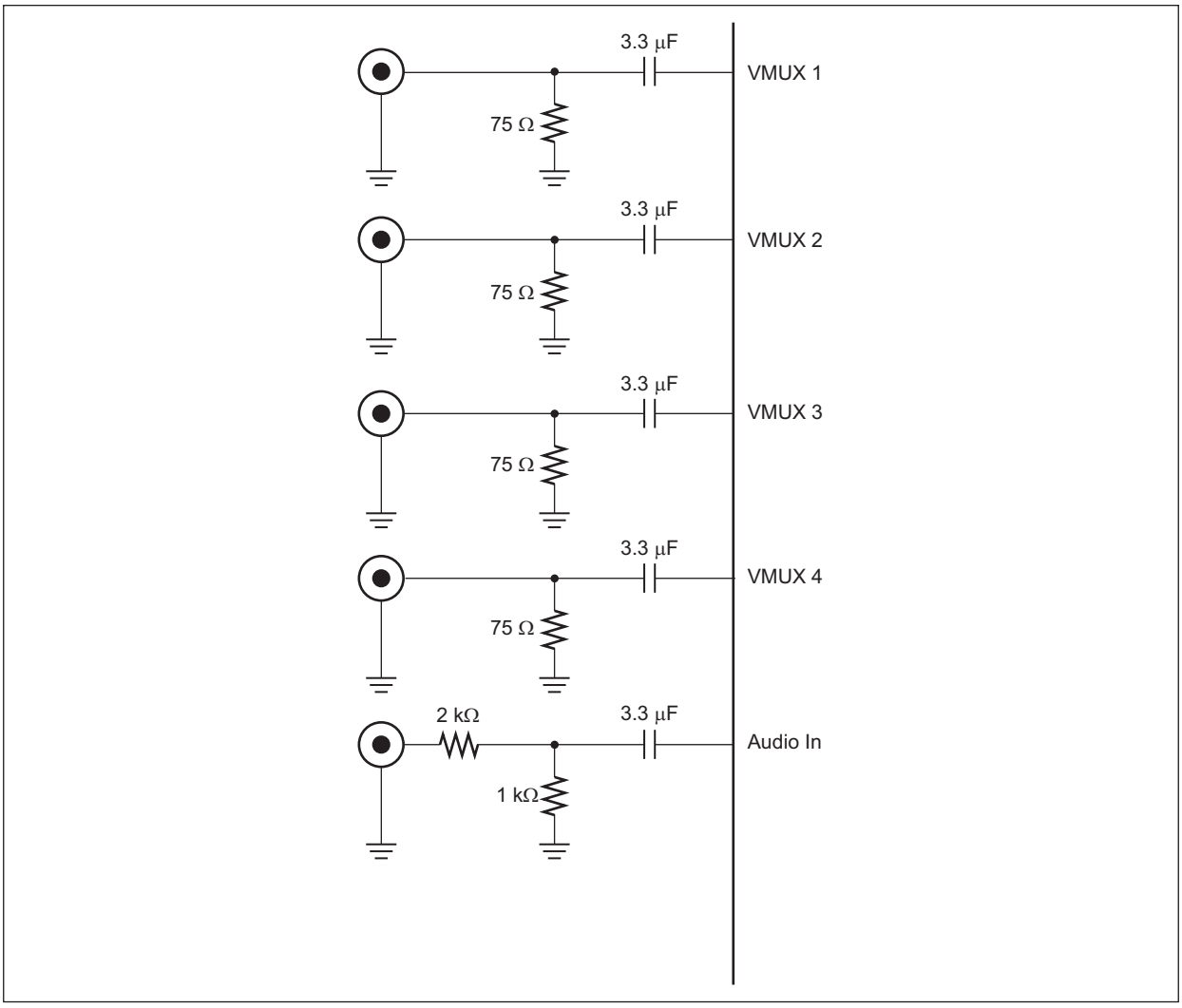
The composite multiplexer is not a break-before-make design. Therefore, during multiplexer switching time, it is possible for the input video signals to be momentarily connected together through the equivalent of 200 Ω. In addition, the multiplexer cannot be switched on a real-time, pixel-by-pixel basis.

3.1.2.1 ADCs

The CX25800 uses two on-chip, 10-bit ADCs to digitize the baseband video signals and audio signals.

The input video and audio signals must be AC-coupled to the decoder. A heavy internal bias current may overheat the device if the input is connected directly to ground. A resistor-divider network provides correct input termination, as illustrated in Figure 65.

Figure 65. Resistor-Divider Network



3.1.3 Power-Up Operation

Upon power-up, the status of the CX25800's registers is indeterminate. The RST signal must be asserted to set the register bits to their default values. Upon reset, the CX25800 defaults to NTSC-M format.

3.1.4 Crystal Inputs and Clock Generation

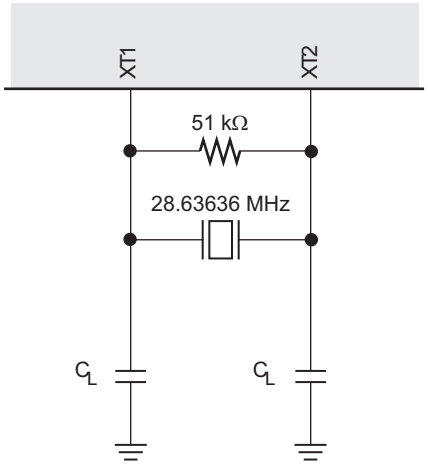
The CX25800 includes an internal Phase Lock Loop (PLL) that can be used to decode NTSC and PAL. The clock signal interface consists of a pair of I/O pins connected to a 28.63636 MHz (8 × NTSC Fsc) crystal. When using the PLL, a 28.63636 MHz, 50 ppm, fundamental (or 3rd overtone) crystal must be connected across XT1 and XT2. Alternately, a single-ended oscillator can be connected to XT1.

Crystals are specified as follows:

- 28.63636 MHz
- Fundamental cut or Third Overtone
- Parallel resonant
- 30 pF load capacitance
- 50 ppm at 25° C
- Series resistance 40 Ω or less

Figure 66, Fundamental Crystal Oscillator, illustrates the fundamental crystal oscillator clock circuit. Figure 67, 3rd Overtone Crystal Oscillator, illustrates the 3rd overtone crystal oscillator clock circuit.

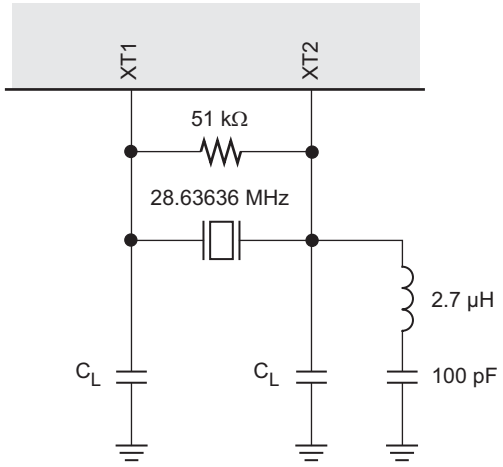
Figure 66. Fundamental Crystal Oscillator



Fundamental Crystal Oscillator

GENERAL NOTE:
Value for C_L varies by crystal manufacturer. Use capacitor recommended by vendor.

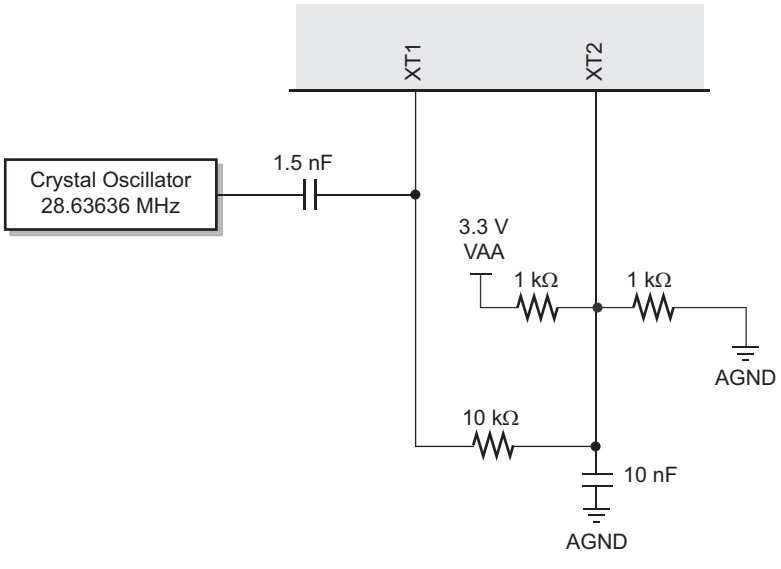
Figure 67. 3rd Overtone Crystal Oscillator



GENERAL NOTE:
Value for C_L varies by crystal manufacturer. Use capacitor recommended by vendor.

The clock source tolerance should be 50 ppm or less. Devices that output CMOS voltage levels are required. The load capacitance in the crystal configurations may vary depending on the magnitude of board parasitic capacitance. The CX25800 is dynamic and, to ensure proper operation, the clocks must always be running with a minimum frequency of 28.63636 MHz.

Figure 68. Crystal Clock Oscillator



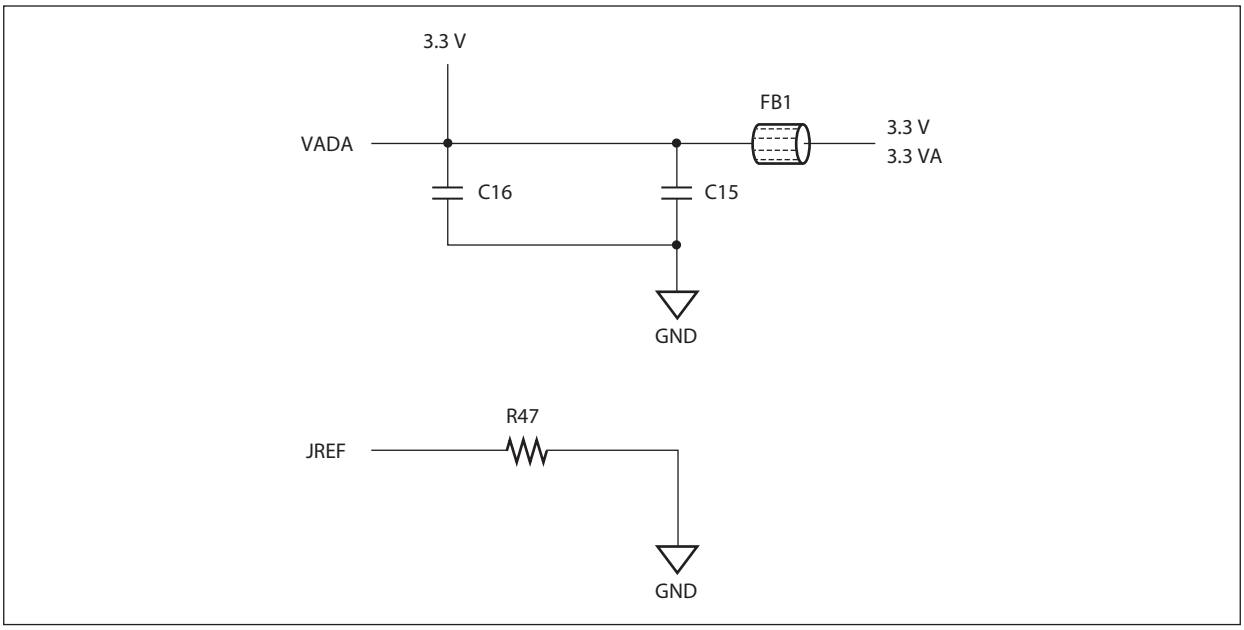
3.1.5 Audio Considerations

Careful attention should be given to VADA DAC source and IREF current DC coupling capacitors to ensure proper audio quality. Proper implementation is illustrated in Figure 69.

In addition, to ensure good audio performance and noise immunity, attention should be given to the following:

- Digital terminating resistors should be connected to digital supplies.
- Components connected to analog pins should be connected to analog ground.
- Analog traces should be routed over analog planes wherever possible.
- Digital traces should be routed over digital planes wherever possible.
- Digital ground should be connected to chassis ground (bottom of the bracket and the connector shields).

Figure 69. Audio Implementation



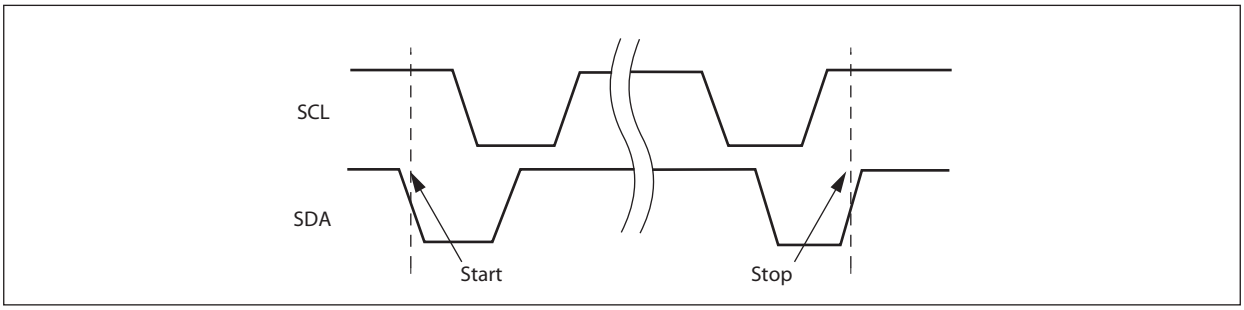
3.2 Serial Bus Interface

The serial bus is a two-wire serial interface that is compatible with the typical two-wire serial interface bus. Serial interface clock and serial interface data signals, SIC and SID, are used to transfer data between the bus master and the slave device. The CX25800 implements the serial bus to support multiple EEPROM devices and other two-wire serial interface devices. Serial bus transfers can be initiated in several ways using the two-wire serial interface Direct, two-wire serial interface Data/Control, or VPD registers. The two-wire serial interface INT bit is set in the PCI Interrupt Status register when a two-wire serial interface operation has completed. This bit can be masked and polled, or be unmasked and used to send an interrupt to the host. The two-wire serial interface can be programmed to run at 100 kHz or 400 kHz.

The two-wire serial interface Direct register is a 15-bit address range that can be used to read and write four consecutive bytes. The upper 7 bits are the two-wire serial interface chip address, and the lower 8 bits are the two-wire serial interface subaddress. The VPD mechanism also can be used to read and write four consecutive bytes, using its 15-bit address range for the two-wire serial interface chip and subaddresses. The two-wire serial interface Data/Control register can be used to perform single and multiple byte transfers using hardware logic. It can also be used to directly provide software control of the two-wire serial interface signals SIC and SID.

The relationship between SIC and SID is decoded to provide both start and stop conditions on the bus. To initiate a transfer on the two-wire serial interface bus, the master must transmit a start pulse to the slave device. This is accomplished by taking the SID signal low while the SIC signal is held high. The master should only generate a start pulse at the beginning of the cycle, or after the transfer of a data byte to or from the slave. To terminate a transfer, the master must take the SID signal high while the SIC signal is held high. The master can issue a stop pulse at any time during a two-wire serial interface cycle. Care must be taken to ensure that data is stable during the high phase of the clock, as the two-wire serial interface bus interprets any transition on the SID signal during the high phase of the SIC signal as a start or stop pulse. This is illustrated in Figure 70, The Relationship Between SIC and SID.

Figure 70. The Relationship Between SIC and SID



A two-wire serial interface write transaction consists of sending a START, two or three bytes of data (checking for a receiver acknowledge after each byte), and a STOP. The write data is supplied by the two-wire serial interface Data/Control register bytes two-wire serial interface DB0, two-wire serial interface DB1, and two-wire serial interface DB2. The least significant bit of two-wire serial interface DB0 is the read/write bit and is low for a write. Two or three bytes of data can be selected for transfer by using the two-wire serial interface W3BRA bit.

A two-wire serial interface read transaction consists of sending a START, one byte of data (checking for a receiver acknowledge), reading one data byte from the slave, sending the master NACK, and sending the STOP. The data read is available in the

two-wire serial interface DB2 byte. The least significant bit of two-wire serial interface DB0 is the read/write bit and is high for a read.

A transaction sequence involving a repeated START usually occurs after setting up a slave read address using a two-byte write transaction, then following with a one-byte read (with one-byte slave address write) transaction. The STOP can be disabled for the first transaction by setting two-wire serial interface NOSTOP high only for the first register write. Two-wire serial interface NOSTOP should be reset during the second register write. This is because every set of two-wire serial interface transactions should begin with a START and end with a STOP (rule applicable to overall transaction set or sequence).

Multiple byte (>3) write transactions enable communication to devices that support auto-incrementing internal addressing. To avoid reset of the internal address sequencer in some devices, a STOP is not transmitted until the very end of the sequence. The first register write should enable a two-byte write transaction with START. Two-wire serial interface NOSTOP should be set to disable STOP temporarily. The SIC signal is held in the low state while the two-wire serial interface DONE interrupt is processed. The second and successive register writes enable one-byte writes to be transmitted without START and without STOP (two-wire serial interface NOS1B and two-wire serial interface NOSTOP both high). The last register write should enable the final STOP to be sent to end the sequential write transaction set. The one-byte write data is sent from two-wire serial interface DB0. The read/write mode was saved from the first register write when the START was transmitted.

For multiple byte (>1) sequential reads, the first register write enables the START and slave address to be transmitted. The first read byte is received into two-wire serial interface DB2. The STOP is disabled through two-wire serial interface NOSTOP. Since the reading continues, the master should ACK at the end of the first read (set two-wire serial interface W3BRA high). The SIC signal is held in the low state while the two-wire serial interface DONE interrupt is processed. The second and successive register writes enables one-byte reads to be received without sending START or STOP (two-wire serial interface NOS1B and two-wire serial interface NOSTOP both high). The last register write should reset E2C_W3BRA low to master NACK. This indicates final read from slave, and enable the final STOP to be sent to end the sequential read transaction set. The one-byte read data is also read from two-wire serial interface DB2. The read/write mode was saved from the first register write when the START was transmitted, so two-wire serial interface DB0 is a don’t-care during one-byte reads.

3.2.1 Serial Bus Serial EEPROM Interface

An external EEPROM is required to support Subsystem ID, function enables, and Vital Product Data (VPD). The EEPROM must reside on the two-wire serial interface bus (SID, SIC).

3.2.2 EEPROM Upload at PCI Reset

The function enables and the 32-bit PCI Subsystem IDs are read from the EEPROM automatically by the hardware immediately following PCI reset deassertion. The function enables are contained in bits[4:1] of the byte at address 15'h5000. Bits 4 through 1 are used for functions 4 through 1, respectively. Function 0 must always be enabled, and therefore has no enable bit. The bytes from 15'h5001-15'h5003 are read, but currently have no meaningful information.

The subsystem ID is contained in 4 bytes of the EEPROM starting at address 15'h5004. To get the subsystem IDs, a read transaction to access the 4 bytes beginning at address 15'h5004 occurs. The subsystem IDs are stored in the EEPROM in the same order as they appear in the PCI configuration space. The full read sequence is detailed in Table 22, EEPROM Read Sequence.

Table 22. EEPROM Read Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	8'hA0		ACK		Write control byte with slave chip address
	8'h00		ACK		Data bytes base address
START	8'hA1		ACK		Read control byte with slave chip address
		8'h??		ACK	
		8'h??		ACK	
		8'h??		ACK	
		8'h??		NACK, STOP	
START	8'hA0		ACK		Write control byte with slave chip address
	8'h04		ACK		Data bytes base address
START	8'hA1		ACK		Read control byte with slave chip address
		8'h??		ACK	Subs Vendor ID [7:0] @ 11'h004
		8'h??		ACK	Subs Vendor ID [15:8] @ 11'h005
		8'h??		ACK	Subsystem ID [7:0] @ 11'h006
		8'h??		NACK, STOP	Subsystem ID [15:8] @ 11'h007
?? represents the unknown actual data that is read from the EEPROM.					

If at any time the slave device issues a NACK (because the device is not present), the sequence is aborted, the enables are all 0, and the Subsystem Vendor IDs read 32'h0000_0000. In this case, function 0 is the only function enabled. Normally it takes approximately 1.3 ms to read these dwords into the PCI configuration register. Any attempted PCI transactions to the CX25800 during this process result in a RETRY.

3.2.3 Register Load from BIOS

The Subsystem ID register is read-only. However, by enabling SVIDS_EN in the user-defined PCI configuration control register, the Subsystem ID can be written. Then SVIDS_EN should be disabled. This value must be programmed before the operating system boots and has access during configuration. This must occur through support from the BIOS versus the IC driver.

3.3 Vital Product Data

VPD is usable by the board manufacturer, system vendor, and the customer. This data is required by *PCI Local Bus Specification Rev 2.3* (for devices after 6/30/98). The VPD format in the EEPROM uses the Large Resource Date type, which allows efficient storage of variable-length data fields. Most of the data is in ASCII format. Each function's VPD is accessed through any of the function's configuration space VPD interface support registers.

3.3.1 Required VPD

A Plug-and-Play compatible product name is the first VPD item. The Product Name large resource type ID string tag field value is 0x82. The tag is followed by a length-of-data word and actual ASCII data. The large resource type VPD-R (tag field value is 0x90) wraps other required read-only VPD field items (keyword): Part Number of Assembly (PN), Field Replaceable Unit Part Number (FN), Engineering Change Level of Assembly (EC), Manufacture ID (MN), Serial Number (SN), and Checksum and Reserved (RV).

3.3.2 VPD Access

The flag bit in the VPD Capability register is used to indicate the transfer of data between the VPD Data register and the EEPROM. To read VPD information a 0 is written to the flag at the same time the 15-bit byte address is supplied to the VPD Address register. The device sets the flag after it reads four bytes from the EEPROM. The four VPD Data register bytes, a dword, correspond to VPD Address+3 … Address+0, or little-endian format. Software monitors the flag to determine the appropriate time to read the VPD Data register. To write data to the R/W portion of the EEPROM, software must write a dword to the VPD Data register, then set the flag bit to a 1 while supplying the VPD Address. When the device completes writing the four bytes to the EEPROM, it resets the flag bit to 0. The VPD Data register is byte accessible. However, all transfers to/from the EEPROM are always 4-byte transactions (except when done with a memory-mapped two-wire serial interface transaction).

3.3.3 VPD Address

The 15-bit logical byte address maps directly to the EEPROM physical storage space. Bits[14:11] must be 4'b1010 to match the defined two-wire serial interface EEPROM chip address, bits[10:8] select one of eight 256 byte spaces, and bits[7:0] is the byte address within the 256 byte space. Addresses 11'h000-11'h007 are reserved in the EEPROM for function enables and Subsystem Vendor ID, therefore the first available VPD address is {4'b1010,3'b000,8'b00001000} (15'h5008). Since all VPD accesses are a full dword, the four bytes use the VPD address as its base.

Table 23. VPD Addresses

VPD Logical Address	Two-Wire Serial Interface Physical Address	EEPROM Usage
15'h07F4	15'h57FC	VPD last DWORD
15'h07F0	15'h57F8	VPD next to last DWORD
—	—	—
—	—	—
—	—	—
15'h0004	15'h500C	VPD second DWORD
15'h0000	15'h5008	VPD first DWORD
	15'h5004	Subsystem ID
	15'h5000	Function Enables

3.3.4 VPD Read

When software resets the VPD flag bit, the CX25800 initiates the two-wire serial interface sequence shown in Table 24, VPD Read Sequence, to read four bytes from the EEPROM (assumes VPD address was set to 15'h5008):

Table 24. VPD Read Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	8'hA0		ACK		Write ctrl byte with slave chip adr
	8'h08		ACK		Data bytes base address
START	8'hA1		ACK		Read ctrl byte with slave chip adr
		8'h??		ACK	VPD[31:24] @ 11'h00B
		8'h??		ACK	VPD[23:16] @ 11'h00A
		8'h??		ACK	VPD[15:8] @ 11'h009
		8'h??		NACK, STOP	VPD[7:0] @ 11'h008
GENERAL NOTES: ?? represents the unknown actual data that is read from the EEPROM.					

NOTE: The device sets the VPD flag bit once all four bytes are read into the VPD data register. If a slave NACK is received, the sequence is aborted, and the flag bit is not set.

3.3.5 VPD Write

When software sets the VPD flag bit, the CX25800 initiates the two-wire serial interface sequence shown in Table 25, VPD Write Sequence, to write four bytes to the EEPROM (assumes VPD address was set to 15'h07F4):

Table 25. VPD Write Sequence

Master		Slave		Master	Comment
Control	Data	Data	Control	Control	
START	8'hAE		ACK		Write ctrl byte with slave chip adr
	8'hFC		ACK		Data bytes base address
	8'h??		ACK		VPD[31:24] @ 11'h7FF
	8'h??		ACK		VPD[23:16] @ 11'h7FE
	8'h??		ACK		VPD[15:8] @ 11'h7FD
	8'h??		ACK	STOP	VPD[7:0] @ 11'h7FC
START	8'hAC		?ACK?	STOP	Loop until ACK, then STOP
GENERAL NOTES: ?? represents the unknown actual data that is read from the EEPROM.					

NOTE: The device resets the VPD flag bit once all four bytes from the VPD data register are programmed into the EEPROM. If a slave NACK is received during either page write, the sequence is aborted, and the flag bit is not reset. Note that a SW time-out on the flag status is the only way to detect an error. It takes approximately 4 ms to program the dword into the EEPROM.

3.4 Power Management Interface

The CX25800 supports power management as outlined in PCI Bus Power Management Interface Specification, revision 1.1. Power management states D0, D3hot, and D3cold are supported. Optional power states D1 and D2 are not supported because there are no significant power savings without going to D3. Restoring a function from D1 to D2 would also require device-specific interaction that the operating system does not currently support.

3.4.1 PME#

The Power Management Even signal PME# is not used because wake-up events are not generated by the CX25800.

3.4.2 D3 Power States

The CX25800 supports D0 (on) and D3cold (off) by default. Each function also supports D3hot independently. When placing a function in D3hot, the operating system is required to disable I/O, memory space, and bus mastering through the PCI Command register. Restoring a function from D3 requires the operating system to reinitialize the function. Full context must be restored before the function is capable of resuming normal operation.

Functions in D3hot respond to configuration space accesses as long as the power and clock are supplied. In addition to each function being disabled from memory access and bus mastering, the D3hot power state enables extra power savings by powering down as many circuits as possible. The video function disables the VFE (sleep ADCs, disable AGC), PLL, and decoder clocks (gate off XTAL signals in CLKIOGEN). The audio function disables its clock and the AFE. In addition, each function resets as many circuits as possible without disabling the configuration access.

3.5 JTAG Interface

3.5.1 Need for Functional Verification

As the complexity of imaging chips increases, the need to easily access individual chips for functional verification is becoming vital. The CX25800 has incorporated special circuitry that allows it to be accessed in full compliance with standards set by the Joint Test Action Group (JTAG). Conforming to IEEE Standard *P1149.1*, "Standard Test Access Port and Boundary Scan Architecture," the CX25800 has dedicated pins that are used for testability purposes only.

3.5.2 JTAG Approach to Testability

The JTAG's approach to testability uses boundary scan cells placed at each digital pin and digital interface. In the CX25800, a digital interface is the boundary between an analog block and a digital block. All cells are interconnected into a boundary scan register that applies or captures test data used for functional verification of the integrated circuit. The JTAG is particularly useful for board testers using functional testing methods.

The JTAG consists of four dedicated pins comprising the Test Access Port (TAP):

- Test Mode Select (TMS)
- Test Clock (TCK)
- Test Data Input (TDI)
- Test Data Out (TDO)

Verification of the integrated circuit and its connection to other modules on the printed circuit board can be achieved through these four TAP pins.

With boundary scan cells at each digital interface and pin, the CX25800 has the capability to apply and capture the respective logic levels. Because all of the digital pins are interconnected as a long shift register, the TAP logic has access and control of all the necessary pins to verify functionality. The TAP controller can shift in any number of test vectors through the TDI input and apply them to the internal circuitry. The output result is scanned out on the TDO pin and externally checked. While isolating the CX25800 from other components on the board, the user has easy access to all digital pins and digital interfaces through the TAP and can perform complete functionality tests without using expensive bed-of-nails testers.

3.5.3 Optional Device ID Register

The CX25800 has the optional device identification register defined by the JTAG specification as listed in Table 26, Device Identification Register. This register contains information concerning the revision, actual part number, and manufacturer's identification code specific to Conexant. This register can be accessed through the TAP controller through an optional JTAG instruction.

Table 26. Device Identification Register

Version				Part Number														Manufacturer ID											
X	X	X	X	0	0	0	0	0	0	1	1	0	1	0	1	0	0	0	0	0	0	0	1	1	0	1	0	1	1	0	1
0				0x036E														0x0D6											
4 Bits				16 Bits														11 Bits											

3.5.4 Verification with the TAP Controller

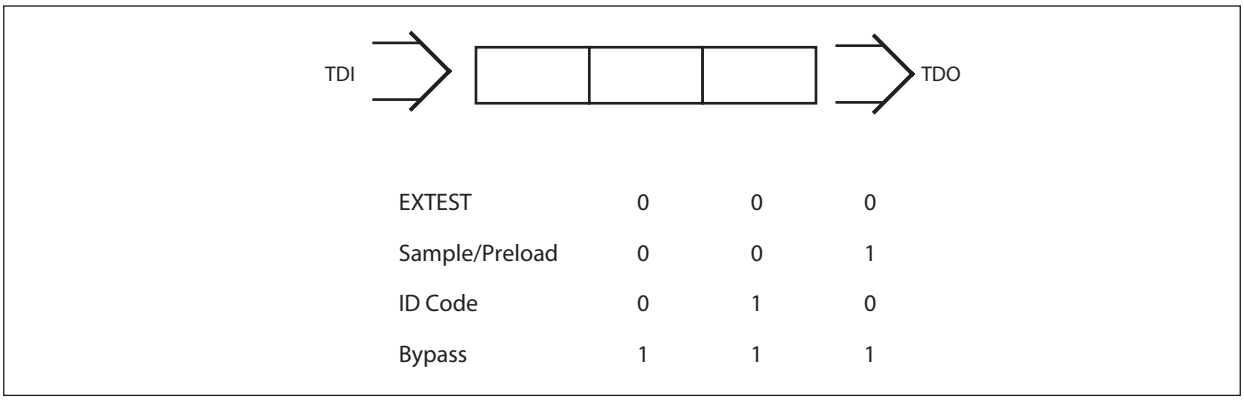
A variety of verification procedures can be performed through the TAP controller. With a set of four instructions, the CX25800 can verify board connectivity at all digital interfaces and pins. The following instructions are accessible by using a state machine standard to all JTAG controllers:

- Sample/Preload
- Extest
- ID Code
- Bypass (see Figure 71, Instruction Register)

Refer to the *IEEE Standard 1149.1* specification for details concerning the Instruction register and JTAG state machine (http://standards.ieee.org/).

Conexant has created a Boundary Scan Descriptive Language (BSDL) with the AT&T BSD™ Editor. For JTAG testing, obtain a disk with an ASCII version of the complete BSDL file by contacting your local Conexant applications engineer.

Figure 71. Instruction Register



4 PC Board Layout Considerations

4.1 Layout Considerations

The PC board layout should be optimized for lowest noise on the CX25800 power and ground lines. Route digital traces away from analog traces. All shields must be connected to the ground plane with a low impedance connection. Use shielded connectors.

4.1.1 Capacitors

Place bypass capacitors (using 0.1 µF ceramic capacitors) close to the CX25800 where possible. Also, whenever possible, place traces from all power pins to a bypass capacitor on the component side in addition to any feedthrough. Finally, place traces from all ground pins to a bypass capacitor on the component side, in addition to any feedthrough, when possible.

Ensure that there is an ample ground plane under the CX25800. Make wide paths of copper under and around the CX25800, if possible. Avoid creating a cut in the plane with feedthroughs, instead, disperse them. Also, ensure that there is an ample power plane under the CX25800.

Fill as follows:

- 2-layer PCB, use ground fill on bottom side.
- 4-layer PCB, no ground fill on top and bottom sides.

4.1.2 Components

Place the following components as close as possible to the CX25800.

- Voltage regulators
- Analog audio filters

5 Registers

CX25800 register types are listed in Table 27.

Table 27. Register Types

Register Type	Description
RO	Read-only
WO	Write-only
R/W	Read/Write
R/W*	Read/Write, but data may not be same as written at a later time (volatile).
RR	Same as R/W, but writing a 1 resets corresponding bit location; writing 0 has no effect.

Unused register bits read back 0.

5.1 PCI Configuration Registers: Function 0: Video

These registers are related to the video function only. Since the CX25800 is a multifunction PCI device, AD[10:8] are used to indicate which function the PCI bus is addressing. This function only responds when AD[10:8] are equal to 3'b000 during a configuration type 0 transaction.

Functions 1–4 share the same physical Device Control register as function 0. The enable/control bits affect all functions. The Subsystem Vendor IDs are also a shared register having read-write access by all functions. There also is one PLL test control register which is accessible by all functions in the PCI configuration space.

Since VPD is required for each function of a multifunction PCI device, VPD for each of the functions can be accessed through the same VPD configuration space mechanism as defined in function 0. Each function's VPD data register interface is through the same flag, address, and data registers. So, it is not possible to start multiple read/write transactions by communicating multiplex to multiple functions (physically impossible given only one EEPROM).

The configuration registers are also mapped into the internal CX25800 memory space for software convenience.

Vendor and Device ID

Register 8'h00—F0_VNDR_DEV_ID_CFG

Register 24'h2F0000—F0_VNDR_DEV_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RO	16'h8800	DEV_ID	DEV_ID = 16'h8800
[15:0]	RO	16'h14F1	VNDR_ID	VNDR_ID = 16'h14F1

Command and Status Register

Register 8'h04—F0_CMD_STAT_CFG

Register 24'h2F0004—F0_CMD_STAT_MM

Bits	Type	Default	Name	Description
[31]	RR	1'b0	PAR_ERR_DET	Set when a parity error is detected in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	1'b0	SYS_ERR	Set when SERR# is asserted.
[29]	RR	1'b0	MSTR_ABRT	Set when master transaction is terminated with Master Abort.
[28]	RR	1'b0	TRGT_ABRT_RCV	Set when master transaction is terminated with Target Abort.
[27]	RO	1'b0	TRGT_ABRT_SIG	Set when target terminates transaction with Target Abort. This bit is always 0, because CX25800 does not respond with a target abort.
[26:25]	RO	2'b01	DEVSEL_TIME	Responds with medium DEVSEL# timing.
[24]	RR	1'b0	MSTR_PAR_ERR	Set when the master asserts PERR# during a read transaction or observes PERR# asserted by target when writing data to target. The Parity Error Response bit in the command register must be enabled.
[23]	RO	1'b1	TRGT_B2B_CAP	CX25800 target is capable of fast back-to-back transactions.
[22]	RO	1'b0	Reserved	Defined as reserved in the PCI specification.
[21]	RO	1'b0	66MHZ_CAP	CX25800 is NOT designed to work at 66 MHz.
[20]	RO	1'b1	CAP_LIST	CX25800 implements a PCI capabilities list, beginning at address offset 8'h34.
[19:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[19]	RO	1'b0	INT_STAT	Reflects the state of the function's interrupt, regardless of the INT_DIS bit.
[18:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[15:11]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.

[15:10]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.
[10]	RW	1'b0	INT_DIS	A value of 1 disables the assertion of the INTA# pin by this function.
[9]	RO	1'b0	MSTR_B2B_CAP	CX25800 master is not capable of fast back-to-back transactions.
[8]	RW	1'b0	SERR#_EN	SERR# driver enable. A value of 1 enables the driver. Address parity errors are reported only if this bit and Parity Error Response bit are 1.
[7]	RO	1'b0	ADR_DATA_STEP	CX25800 does not do address or data stepping.
[6]	RW	1'b0	PAR_ERR_RSP	A value of 1 enables parity error reporting.
[5]	RO	1'b0	VGA_SNP	CX25800 does not snoop VGA palette accesses.
[4]	RW	1'b0	MEM_WR_INV_EN	CX25800 does not use memory write and invalidate command, so does not need this enable.
[3]	RO	1'b0	SPCL_CYCL_EN	CX25800 does not use special cycles.
[2]	RW	1'b0	MSTR_EN	A value of 1 allows CX25800 to behave as a master.
[1]	RW	1'b0	MEM_RSP	A value of 1 allows CX25800 to respond to memory space accesses.
[0]	RO	1'b0	IO_RSP	CX25800 has no I/O address space.

Revision ID and Class Code

Register 8'h08—F0_REVID_CLASS_CFG

Register 24'h2F0008—F0_REVID_CLASS_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'h040000	CLASS_CODE	This CX25800 video function is a multimedia video device.
[7:0]	RO	8'hxx	REV_ID	This register identifies the device revision.

Cache Line Size, Latency Timer, Header Type, BIST

Register 8'h0C—F0_LN_LAT_HDR_CFG

Register 24'h2F000C—F0_LN_LAT_HDR_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	BIST	CX25800 does not implement this BIST function.
[23:16]	RO	8'h80	HDR_TYPE	CX25800 is a multifunction PCI device.
[15:8]	RW	8'h00	LAT_TIMER	The number of PCI bus clocks for the latency timer used by the master for this function. Once the latency expires, the master initiates transaction termination as soon as GNT# is removed.
[7:0]	RW	8'h00	CACHE_LN_SZ	System software loads this with the system cache line size. This information is used by the masters using Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple.

Base Address 0

Register 8'h10—F0_BAR0_CFG

Register 24'h2F0010—F0_BAR0_MM

Bits	Type	Default	Name	Description
[31:24]	RW	8'h00	BASE_ADRS_UPR	These upper bits are written by the system software to locate the function registers in the PCI address space.
[23:0]	RO	24'h000000	BASE_ADRS_LWR	These lower bits indicate to the system software that 16 MB of nonprefetchable data are required anywhere in the 32-bit memory address space.

Subsystem Vendor and Subsystem ID

Register 8'h2C—F0_SUBSYS_ID_CFG

Register 24'h2F002C—F0_SUBSYS_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RW	16'h0000	SUBSYS_ID	This is automatically loaded at reset with the value from addresses 12'h006 (least significant byte) and 12'h007 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.
[15:0]	RW	16'h0000	SUBSYS_VNDR_ID	This is automatically loaded at reset with the value from addresses 12'h004 (least significant byte) and 12'h005 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.

Capabilities Pointer

Register 8'h34—F0_CAP_PTR_CFG

Register 24'h2F0034—F0_CAP_PTR_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'b0	Reserved	Defined as reserved in the PCI specification.
[7:0]	RO	8'h4C	CAP_PTR	Dword-aligned byte address offset in configuration space to the first item in the list of capabilities.

Interrupt Line, Interrupt Pin, Minimum Grant, Maximum Latency

Register 8'h3C—F0_INT_GNT_LAT_CFG

Register 24'h2F003C—F0_INT_GNT_LAT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h37	MAX_LAT	Require bus access every 13.9 ms, in units of 250 ns. Affects the setting for the latency timer.
[23:16]	RO	8'h14	MIN_GNT	Desire a minimum grant burst period of 5 ms, in units of 250 ns. Affects the setting for the latency timer.
[15:8]	RO	8'h01	INT_PIN	CX25800 interrupt pin is connected to INTA#.
[7:0]	RW	8'h00	INT_LINE	The interrupt line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the CX25800 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Device Control #1

Register 8'h40—F0_DEV_CNTRL1_CFG

Register 24'h2F0040—F0_DEV_CNTRL1_MM

Register 32'hxx2F0040—F0_DEV_CNTRL1_MM

Bits	Type	Default	Name	Description
[31:29]	RO	11'b0	Reserved	
[28]	RW	1'b1	FNC4_EN	When 1, this function is enabled. When 0, it is disabled. This bit is loaded from EEPROM automatically when PCI reset is deasserted. The R/W accessibility is for test purposes only.
[27]	RW	1'b1	FNC3_EN	Same as bit 28 above
[26]	RW	1'b1	FNC2_EN	Same as bit 28 above
[25]	RW	1'b1	FNC1_EN	Same as bit 28 above
[24]	RO	1'b1	FNC0_EN	Same as bit 28 above, except there is no write allowed. PCI function 0 may not be disabled.
[20]	RW	1'b1	Two-wire serial interface RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[19]	RW	1'b1	GPHST_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[18]	RW	1'b1	VIP_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[17]	RW	1'b1	AUD_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.

[16]	RW	1'b1	VID_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[12]	RW	1'b1	Two-wire serial interface RDY_EN	When 1, the ready and transfer-in-progress logic for the two-wire serial interface is enabled. When 0, the logic is disabled. In this case, the two-wire serial interface XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[11]	RW	1'b1	GPHST_RDY_EN	When 1, the ready and transfer-in-progress logic for General Purpose Host is enabled. When 0, the logic is disabled. In this case, the GPHST_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[10]	RW	1'b1	VIP_RDY_EN	When 1, the ready and transfer-in-progress logic for VIP is enabled. When 0, the logic is disabled. In this case, the VIP_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[9]	RW	1'b1	AUD_RDY_EN	When 1, the ready and transfer-in-progress logic for audio is enabled. When 0, the logic is disabled. In this case, the AUD_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[8]	RW	1'b1	VID_RDY_EN	When 1, the ready and transfer-in-progress logic for video is enabled. When 0, the logic is disabled. In this case, the VID_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[6:4]	RW	3'b011	DMA_RTRY_LMT	Selects the number of retries that are allowed before the DMA arbiter switches to the other channel.
[3]	RW	1'b0	EN_VSFX	Enable VIA/SIS PCI controller compatibility mode for all functions 0, 1, 2, 3, and 4.
[0]	RW	1'b0	SVIDS_EN	A value of 1 enables writes to the Subsystem and Subsystem Vendor ID register for all functions 0, 1, 2, 3, and 4.

VPD Capability

Register 8’h44—F0_VPD_CAP_CFG

Register 24’h2F0044—F0_VPD_CAP_MM

Bits	Type	Default	Name	Description
[31]	RW	1’b0	VPD_Flag	This flag is set to 1 when the device completes reading and transfer of four bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW	15’b0	VPD_ADRS	Logical byte address of the VPD to be accessed.
[15:8]	RO	8’h4C	VPD_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8’h03	VPD_ID	VPD new capability data structure ID assigned by SIG.

VPD Data

Register 8’h48—F0_VPD_DATA_CFG

Register 24’h2F0048—F0_VPD_DATA_MM

Bits	Type	Default	Name	Description
[31:0]	RW*	32’b0	VPD_DATA	Four bytes are always transferred between the VPD data register and the EEPROM. The LSB…MSB is transferred from/to VPD_ADRS…VPD_ADRS+3.

Power Management Capability

Register 8'h4C—F0_PWR_MAN_CAP_CFG

Register 24'h2F004C—F0_PWR_MAN_CAP_MM

Bits	Type	Default	Name	Description
[31:27]	RO	5'b00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	1'b0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	1'b0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	3'b000		Reserved
[21]	RO	1'b1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	1'b0		Reserved
[19]	RO	1'b0	PMC_PME_CLK	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	3'b010	PMC_VRSN	Function complies with version 1.1 of the PCI Power Management Specification.
[15:8]	RO	8'h00	PMC_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8'h01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

Power Management Support Registers

Register 8'h50—F0_PWR_MAN_SPRT_CFG

Register 24'h2F0050—F0_PWR_MAN_SPRT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	PWR_DATA	This field is used to report the state dependent data requested by DATA_SEL and scaled by DATA_SCALE. Optional and not supported.
[23:16]	RO	8'h00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	1'b0	PME_STATUS	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	2'b00	DATA _SCALE	This field indicates the scaling factor to be used when interpreting the value of the PWR_DATA register. Optional and not supported.
[12:9]	RO	4'h0	DATA_SEL	This field selects which data is to be reported through the PWR_DATA register. Optional and not supported.
[8]	RO	1'b0	PME_EN	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	6'h00		Reserved
[1:0]	RW	2'b00	PWR_STATE	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

Bits [15:0] are also known as the Power Management Control/Status register or PMCSR. Attempting to set PowerState to D1 or D2 results in no change of state for that 2-bit field.

5.2 PCI Configuration Registers: Function 1: Audio

These registers are related to the audio function only. Since the CX25800 is a multifunction PCI device, AD[10:8] are used to indicate which function the PCI bus is addressing. This function only responds when AD[10:8] are equal to 3'b001 during a configuration type 0 transaction.

Vendor and Device ID

Register 8'h00—F1_VNDR_DEV_ID_CFG

Register 24'h2F0100—F1_VNDR_DEV_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RO	16'h8801	DEV_ID	DEV_ID = 16'h8801
[15:0]	RO	16'h14F1	VNDR_ID	VNDR_ID = 16'h14F1

Command and Status Register

Register 8'h04—F1_CMD_STAT_CFG

Register 24'h2F0104—F1_CMD_STAT_MM

Bits	Type	Default	Name	Description
[31]	RR	1'b0	PAR_ERR_DET	Set when a parity error is detected in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	1'b0	SYS_ERR	Set when SERR# is asserted.
[29]	RR	1'b0	MSTR_ABRT	Set when master transaction is terminated with Master Abort.
[28]	RR	1'b0	TRGT_ABRT_RCV	Set when master transaction is terminated with Target Abort.
[27]	RO	1'b0	TRGT_ABRT_SIG	Set when target terminates transaction with Target Abort. This bit is always 0, as CX25800 does not respond with a target abort.
[26:25]	RO	2'b01	DEVSEL_TIME	Responds with medium DEVSEL# timing.
[24]	RR	1'b0	MSTR_PAR_ERR	Set when the master asserts PERR# during a read transaction or observes PERR# asserted by target when writing data to target. The Parity Error Response bit in the command register must be enabled.
[23]	RO	1'b1	TRGT_B2B_CAP	CX25800 target is capable of fast back-to-back transactions.
[22]	RO	1'b0	Reserved	Defined as reserved in the PCI specification.

[21]	RO	1'b0	66MHZ_CAP	CX25800 is *not* designed to work at 66 MHz.
[20]	RO	1'b1	CAP_LIST	CX25800 implements a PCI capabilities list, beginning at address offset 8'h34.
[19:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[15:10]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.
[9]	RO	1'b0	MSTR_B2B_CAP	CX25800 master is not capable of fast back-to-back transactions.
[8]	RW	1'b0	SERR#_EN	SERR# driver enable. A value of 1 enables the driver. Address parity errors are reported only if this bit and Parity Error Response bit are 1.
[7]	RO	1'b0	ADR_DATA_STEP	CX25800 does not do address or data stepping.
[6]	RW	1'b0	PAR_ERR_RSP	A value of 1 enables parity error reporting.
[5]	RO	1'b0	VGA_SNP	CX25800 does not snoop VGA palette accesses.
[4]	RW	1'b0	MEM_WR_INV_EN	CX25800 does not use memory write and invalidate command, so does not need this enable.
[3]	RO	1'b0	SPCL_CYCL_EN	CX25800 does not use special cycles.
[2]	RW	1'b0	MSTR_EN	A value of 1 allows CX25800 to behave as a master.
[1]	RW	1'b0	MEM_RSP	A value of 1 allows CX25800 to respond to memory space accesses.
[0]	RO	1'b0	IO_RSP	CX25800 has no I/O address space.

Revision ID and Class Code

Register 8’h08—F1_REVID_CLASS_CFG

Register 24’h2F0108—F1_REVID_CLASS_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24’h048000	CLASS_CODE	This CX25800 audio function is a multimedia other device.
[7:0]	RO	8’h04	REV_ID	This register identifies the device revision.

Cache Line Size, Latency Timer, Header Type, BIST

Register 8’h0C—F1_LN_LAT_HDR_CFG

Register 24’h2F010C—F1_LN_LAT_HDR_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8’h00	BIST	CX25800 does not implement this BIST function.
[23:16]	RO	8’h80	HDR_TYPE	CX25800 is a multifunction PCI device.
[15:8]	RW	8’h00	LAT_TIMER	The number of PCI bus clocks for the latency timer used by the master for this function. Once the latency expires, the master initiates transaction termination as soon as GNT# is removed.
[7:0]	RW	8’h00	CACHE_LN_SZ	System software loads this with the system cache line size. This information is used by the masters using Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple.

Base Address 0

Register 8’h10—F1_BAR0_CFG

Register 24’h2F0110—F1_BAR0_MM

Bits	Type	Default	Name	Description
[31:24]	RW	8’h00	BASE_ADRS_UPR	These upper bits are written by the system software to locate the function registers in the PCI address space.
[23:0]	RO	24’h000000	BASE_ADRS_LWR	These lower bits indicate to the system software that 16 MB of nonprefetchable data are required anywhere in the 32-bit memory address space.

Subsystem Vendor and Subsystem ID

Register 8'h2C—F1_SUBSYS_ID_CFG

Register 24'h2F012C—F1_SUBSYS_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RW	16'h0000	SUBSYS_ID	This is automatically loaded at reset with the value from addresses 12'h006 (least significant byte) and 12'h007 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.
[15:0]	RW	16'h0000	SUBSYS_VNDR_ID	This is automatically loaded at reset with the value from addresses 12'h004 (least significant byte) and 12'h005 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.

Capabilities Pointer

Register 8'h34—F1_CAP_PTR_CFG

Register 24'h2F0134—F1_CAP_PTR_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'b0	Reserved	Defined as reserved in the PCI specification.
[7:0]	RO	8'h4C	CAP_PTR	Dword-aligned byte address offset in configuration space to the first item in the list of capabilities.

Interrupt Line, Interrupt Pin, Minimum Grant, Maximum Latency

Register 8'h3C—F1_INT_GNT_LAT_CFG

Register 24'h2F013C—F1_INT_GNT_LAT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'hFF	MAX_LAT	Require bus access every 64 ms, in units of 250 ns. The audio can actually tolerate up to 148.9 ms latency, so the maximum value for this parameter is used. Affects the setting for the latency timer.
[23:16]	RO	8'h04	MIN_GNT	Desire a minimum grant burst period of 1 ms, in units of 250 ns. Affects the setting for the latency timer.
[15:8]	RO	8'h01	INT_PIN	CX25800 interrupt pin is connected to INTA#.
[7:0]	RW	8'h00	INT_LINE	The interrupt line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the CX25800 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Device Control #1

Register 8'h40—F1_DEV_CNTRL1_CFG

Register 24'h2F0140—F1_DEV_CNTRL1_MM

Bits	Type	Default	Name	Description
[31:29]	RO	11'b0	Reserved	
[28]	RW	1'b1	FNC4_EN	When 1, this function is enabled. When 0, it is disabled. This bit is loaded from EEPROM automatically when PCI reset is deasserted. The R/W accessibility is for test purposes only.
[27]	RW	1'b1	FNC3_EN	Same as bit 28 above
[26]	RW	1'b1	FNC2_EN	Same as bit 28 above
[25]	RW	1'b1	FNC1_EN	Same as bit 28 above
[24]	RO	1'b1	FNC0_EN	Same as bit 28 above, except there is no write allowed. PCI function 0 cannot be disabled.
[20]	RW	1'b1	Two-wire serial interface RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[19]	RW	1'b1	GPHST_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[18]	RW	1'b1	VIP_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[17]	RW	1'b1	AUD_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[16]	RW	1'b1	VID_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.

[12]	RW	1'b1	Two-wire serial interface RDY_EN	When 1, the ready and transfer-in-progress logic for the two-wire serial interface is enabled. When 0, the logic is disabled. In this case, the two-wire serial interface XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[11]	RW	1'b1	GPHST_RDY_EN	When 1, the ready and transfer-in-progress logic for General Purpose Host is enabled. When 0, the logic is disabled. In this case, the GPHST_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[10]	RW	1'b1	VIP_RDY_EN	When 1, the ready and transfer-in-progress logic for VIP is enabled. When 0, the logic is disabled. In this case, the VIP_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[9]	RW	1'b1	AUD_RDY_EN	When 1, the ready and transfer-in-progress logic for audio is enabled. When 0, the logic is disabled. In this case, the AUD_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[8]	RW	1'b1	VID_RDY_EN	When 1, the ready and transfer-in-progress logic for video is enabled. When 0, the logic is disabled. In this case, the VID_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[6:4]	RW	3'b011	DMA_RTRY_LMT	Selects the number of retries that are allowed before the DMA arbiter switches to the other channel.
[3]	RW	1'b0	EN_VSFX	Enable VIA/SIS PCI controller compatibility mode for all functions 0, 1, 2, 3, and 4.
[0]	RW	1'b0	SVIDS_EN	A value of 1 enables writes to the Subsystem and Subsystem Vendor ID register for all functions 0, 1, 2, 3, and 4.

VPD Capability

Register 8’h44—F1_VPD_CAP_CFG

Register 24’h2F0144—F1_VPD_CAP_MM

Bits	Type	Default	Name	Description
[31]	RW	1’b0	VPD_Flag	This flag is set to a value of 1 when the device completes reading and transfer of four bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW		VPD_ADRS	Logical byte address of the VPD to be accessed.
[15:8]	RO	8’h4C	VPD_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8’h03	VPD_ID	VPD new capability data structure ID assigned by SIG.

VPD Data

Register 8’h48—F1_VPD_DATA_CFG

Register 24’h2F0148—F1_VPD_DATA_MM

Bits	Type	Default	Name	Description
[31:0]	RW*		VPD_DATA	Four bytes are always transferred between the VPD data register and the EEPROM. The LSB…MSB is transferred from/to VPD_ADRS…VPD_ADRS+3.

Power Management Capability

Register 8'h4C—F1_PWR_MAN_CAP_CFG

Register 24'h2F014C—F1_PWR_MAN_CAP_MM

Bits	Type	Default	Name	Description
[31:27]	RO	5'b00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	1'b0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	1'b0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	3'b000		Reserved
[21]	RO	1'b1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	1'b0		Reserved
[19]	RO	1'b0	PMC_PME_CLK	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	3'b010	PMC_VRSN	Function complies with version 1.1 of the PCI Power Management Specification.
[15:8]	RO	8'h00	PMC_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8'h01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

Power Management Support Registers

Register 8'h50—F1_PWR_MAN_SPRT_CFG

Register 24'h2F0150—F1_PWR_MAN_SPRT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	PWR_DATA	This field is used to report the state dependent data requested by DATA_SEL and scaled by DATA_SCALE. Optional and not supported.
[23:16]	RO	8'h00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	1'b0	PME_STATUS	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	2'b00	DATA _SCALE	This field indicates the scaling factor to be used when interpreting the value of the PWR_DATA register. Optional and not supported.
[12:9]	RO	4'h0	DATA_SEL	This field selects which data is to be reported through the PWR_DATA register. Optional and not supported.
[8]	RO	1'b0	PME_EN	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	6'h00		Reserved
[1:0]	RW	2'b00	PWR_STATE	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

Bits [15:0] are also known as the Power Management Control/Status register or PMCSR. Attempting to set PowerState to D1 or D2 result in no change of state for that 2-bit field.

5.3 PCI Configuration Registers: Function 2: MPEG TS

These registers are related to the MPEG Transport Stream function only. Since CX25800 is a multifunction PCI device, AD[10:8] are used to indicate which function the PCI bus is addressing. This function only responds when AD[10:8] are equal to 3'b010 during a configuration type 0 transaction.

Vendor and Device ID

Register 8'h00—F2_VNDR_DEV_ID_CFG

Register 24'h2F0200—F2_VNDR_DEV_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RO	16'h8802	DEV_ID	DEV_ID = 16'h8802
[15:0]	RO	16'h14F1	VNDR_ID	VNDR_ID = 16'h14F1

Command and Status Register

Register 8'h04—F2_CMD_STAT_CFG

Register 24'h2F0204—F2_CMD_STAT_MM

Bits	Type	Default	Name	Description
[31]	RR	1'b0	PAR_ERR_DET	Set when a parity error is detected in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	1'b0	SYS_ERR	Set when SERR# is asserted.
[29]	RR	1'b0	MSTR_ABRT	Set when master transaction is terminated with Master Abort.
[28]	RR	1'b0	TRGT_ABRT_RCV	Set when master transaction is terminated with Target Abort.
[27]	RO	1'b0	TRGT_ABRT_SIG	Set when target terminates transaction with Target Abort. This bit is always 0 because CX25800 does not respond with a target abort.
[26:25]	RO	2'b01	DEVSEL_TIME	Responds with medium DEVSEL# timing.
[24]	RR	1'b0	MSTR_PAR_ERR	Set when the master asserts PERR# during a read transaction or observes PERR# asserted by target when writing data to target. The Parity Error Response bit in the command register must be enabled.
[23]	RO	1'b1	TRGT_B2B_CAP	CX25800 target is capable of fast back-to-back transactions.
[22]	RO	1'b0	Reserved	Defined as reserved in the PCI specification.
[21]	RO	1'b0	66MHZ_CAP	CX25800 is NOT designed to work at 66 MHz.
[20]	RO	1'b1	CAP_LIST	CX25800 implements a PCI capabilities list, beginning at address offset 8'h34.

[19]	RO	1'b0	INT_STAT	Reflects the state of the function's interrupt, regardless of the INT_DIS bit.
[19:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[15:11]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.
[10]	RW	1'b0	INT_DIS	A value of 1 disables the assertion of the INTA# pin by this function.
[9]	RO	1'b0	MSTR_B2B_CAP	CX25800 master is not capable of fast back-to-back transactions.
[8]	RW	1'b0	SERR#_EN	SERR# driver enable. A value of 1 enables the driver. Address parity errors are reported only if this bit and Parity Error Response bit are 1.
[7]	RO	1'b0	ADR_DATA_STEP	CX25800 does not do address or data stepping.
[6]	RW	1'b0	PAR_ERR_RSP	A value of 1 enables parity error reporting.
[5]	RO	1'b0	VGA_SNP	CX25800 does not snoop VGA palette accesses.
[4]	RW	1'b0	MEM_WR_INV_EN	CX25800 does not use memory write and invalidate command, so does not need this enable.
[3]	RO	1'b0	SPCL_CYCL_EN	CX25800 does not use special cycles.
[2]	RW	1'b0	MSTR_EN	A value of 1 allows CX25800 to behave as a master.
[1]	RW	1'b0	MEM_RSP	A value of 1 allows CX25800 to respond to memory space accesses.
[0]	RO	1'b0	IO_RSP	CX25800 has no I/O address space.

Revision ID and Class Code

Register 8'h08—F2_REVID_CLASS_CFG

Register 24'h2F0208—F2_REVID_CLASS_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'h048000	CLASS_CODE	This CX25800 MPEG transport stream interface function is a multimedia other device.
[7:0]	RO	8'h04	REV_ID	This register identifies the device revision.

Cache Line Size, Latency Timer, Header Type, BIST

Register 8'h0C—F2_LN_LAT_HDR_CFG

Register 24'h2F020C—F2_LN_LAT_HDR_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	BIST	CX25800 does not implement this BIST function.
[23:16]	RO	8'h80	HDR_TYPE	CX25800 is a multifunction PCI device.
[15:8]	RW	8'h00	LAT_TIMER	The number of PCI bus clocks for the latency timer used by the master for this function. Once the latency expires, the master initiates transaction termination as soon as GNT# is removed.
[7:0]	RW	8'h00	CACHE_LN_SZ	System software loads this with the system cache line size. This information is used by the masters using Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple.

Base Address 0

Register 8'h10—F2_BAR0_CFG

Register 24'h2F0210—F2_BAR0_MM

Bits	Type	Default	Name	Description
[31:24]	RW	8'h00	BASE_ADRS_UPR	These upper bits are written by the system software to locate the function3 registers in the PCI address space.
[23:0]	RO	24'h000000	BASE_ADRS_LWR	These lower bits indicate to the system software that 16 MB of nonprefetchable data are required anywhere in the 32-bit memory address space.

Subsystem Vendor and Subsystem ID

Register 8'h2C—F2_SUBSYS_ID_CFG

Register 24'h2F022C—F2_SUBSYS_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RW	16'h0000	SUBSYS_ID	This is automatically loaded at reset with the value from addresses 12'h006 (least significant byte) and 12'h007 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.
[15:0]	RW	16'h0000	SUBSYS_VNDR_ID	This is automatically loaded at reset with the value from addresses 12'h004 (least significant byte) and 12'h005 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.

Capabilities Pointer

Register 8'h34—F2_CAP_PTR_CFG

Register 24'h2F0234—F2_CAP_PTR_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'b0	Reserved	Defined as reserved in the PCI specification.
[7:0]	RO	8'h4C	CAP_PTR	Dword-aligned byte address offset in configuration space to the first item in the list of capabilities.

Interrupt Line, Interrupt Pin, Minimum Grant, Maximum Latency

Register 8'h3C—F2_INT_GNT_LAT_CFG

Register 24'h2F023C—F2_INT_GNT_LAT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h58	MAX_LAT	Require bus access every 22.2 ms, in units of 250 ns. Affects the setting for the latency timer.
[23:16]	RO	8'h06	MIN_GNT	Desire a minimum grant burst period of 1.5 ms, in units of 250 ns. Affects the setting for the latency timer.
[15:8]	RO	8'h01	INT_PIN	CX25800 interrupt pin is connected to INTA#.
[7:0]	RW	8'h00	INT_LINE	The interrupt line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the CX25800 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Device Control #1

Register 8'h40—F2_DEV_CNTRL1_CFG

Register 24'h2F0240—F2_DEV_CNTRL1_MM

Bits	Type	Default	Name	Description
[31:29]	RO	11'b0	Reserved	
[28]	RW	1'b1	FNC4_EN	When 1, this function is enabled. When 0, it is disabled. This bit is loaded from EEPROM automatically when PCI reset is deasserted. The R/W accessibility is for test purposes only.
[27]	RW	1'b1	FNC3_EN	Same as bit 28 above
[26]	RW	1'b1	FNC2_EN	Same as bit 28 above
[25]	RW	1'b1	FNC1_EN	Same as bit 28 above
[24]	RO	1'b1	FNC0_EN	Same as bit 28 above, except there is no write allowed. PCI function 0 may not be disabled.
[20]	RW	1'b1	Two-wire serial interface RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[19]	RW	1'b1	GPHST_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[18]	RW	1'b1	VIP_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[17]	RW	1'b1	AUD_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[16]	RW	1'b1	VID_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[12]	RW	1'b1	Two-wire serial interface RDY_EN	When 1, the ready and transfer-in-progress logic for the two-wire serial interface is enabled. When 0, the logic is disabled. In this case, the two-wire serial interface XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.

[11]	RW	1'b1	GPHST_RDY_EN	When 1, the ready and transfer-in-progress logic for General Purpose Host is enabled. When 0, the logic is disabled. In this case, the GPHST_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[10]	RW	1'b1	VIP_RDY_EN	When 1, the ready and transfer-in-progress logic for VIP is enabled. When 0, the logic is disabled. In this case, the VIP_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[9]	RW	1'b1	AUD_RDY_EN	When 1, the ready and transfer-in-progress logic for audio is enabled. When 0, the logic is disabled. In this case, the AUD_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[8]	RW	1'b1	VID_RDY_EN	When 1, the ready and transfer-in-progress logic for video is enabled. When 0, the logic is disabled. In this case, the VID_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[6:4]	RW	3'b011	DMA_RTRY_LMT	Selects the number of retries that are allowed before the DMA arbiter switches to the other channel.
[3]	RW	1'b0	EN_VSFX	Enable VIA/SIS PCI controller compatibility mode for all functions 0, 1, 2, 3, and 4.
[0]	RW	1'b0	SVIDS_EN	A value of 1 enables writes to the Subsystem and Subsystem Vendor ID register for all functions 0, 1, 2, 3, and 4.

VPD Capability

Register 8’h44—F2_VPD_CAP_CFG

Register 24’h2F0244—F2_VPD_CAP_MM

Bits	Type	Default	Name	Description
[31]	RW	1’b0	VPD_Flag	This flag is set to a value of 1 when the device completes reading and transfer of four bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW		VPD_ADRS	Logical byte address of the VPD to be accessed.
[15:8]	RO	8’h4C	VPD_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8’h03	VPD_ID	VPD new capability data structure ID assigned by SIG.

VPD Data

Register 8’h48—F2_VPD_DATA_CFG

Register 24’h2F0248—F2_VPD_DATA_MM

Bits	Type	Default	Name	Description
[31:0]	RW*		VPD_DATA	Four bytes are always transferred between the VPD data register and the EEPROM. The LSB…MSB is transferred from/to VPD_ADRS…VPD_ADRS+3.

Power Management Capability

Register 8'h4C—F2_PWR_MAN_CAP_CFG

Register 24'h2F024C—F2_PWR_MAN_CAP_MM

Bits	Type	Default	Name	Description
[31:27]	RO	5'b00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	1'b0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	1'b0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	3'b000		Reserved
[21]	RO	1'b1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	1'b0		Reserved
[19]	RO	1'b0	PMC_PME_CLK	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	3'b010	PMC_VRSN	Function complies with version 1.1 of the PCI Power Management Specification.
[15:8]	RO	8'h00	PMC_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8'h01	PMC_ID	PCI Power Management, a new capability data structure ID assigned by SIG.

Power Management Support Registers

Register 8'h50—F2_PWR_MAN_SPRT_CFG

Register 24'h2F0250—F2_PWR_MAN_SPRT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	PWR_DATA	This field is used to report the state dependent data requested by DATA_SEL and scaled by DATA_SCALE. Optional and not supported.
[23:16]	RO	8'h00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	1'b0	PME_STATUS	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	2'b00	DATA _SCALE	This field indicates the scaling factor to be used when interpreting the value of the PWR_DATA register. Optional and not supported.
[12:9]	RO	4'h0	DATA_SEL	This field selects which data is to be reported through the PWR_DATA register. Optional and not supported.
[8]	RO	1'b0	PME_EN	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	6'h00		Reserved
[1:0]	RW	2'b00	PWR_STATE	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

Bits [15:0] are also known as the Power Management Control/Status register or PMCSR. Attempting to set PowerState to D1 or D2 results in no change of state for that 2-bit field.

5.4 PCI Configuration Registers: Function 3: VIP

These registers are related to the VIP Host Master function only. Since the CX25800 is a multifunction PCI device, AD[10:8] are used to indicate which function the PCI bus is addressing. This function only responds when AD[10:8] are equal to 3'b011 during a configuration type 0 transaction.

Vendor and Device ID

Register 8'h00—F3_VNDR_DEV_ID_CFG

Register 24'h2F0300—F3_VNDR_DEV_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RO	16'h8803	DEV_ID	DEV_ID = 16'h8803
[15:0]	RO	16'h14F1	VNDR_ID	VNDR_ID = 16'h14F1

Command and Status Register

Register 8'h04—F3_CMD_STAT_CFG

Register 24'h2F0304—F3_CMD_STAT_MM

Bits	Type	Default	Name	Description
[31]	RR	1'b0	PAR_ERR_DET	Set when a parity error is detected in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	1'b0	SYS_ERR	Set when SERR# is asserted.
[29]	RR	1'b0	MSTR_ABRT	Set when master transaction is terminated with Master Abort.
[28]	RR	1'b0	TRGT_ABRT_RCV	Set when master transaction is terminated with Target Abort.
[27]	RO	1'b0	TRGT_ABRT_SIG	Set when target terminates transaction with Target Abort. This bit is always 0 as CX25800 does not respond with a target abort.
[26:25]	RO	2'b01	DEVSEL_TIME	Responds with medium DEVSEL# timing.
[24]	RR	1'b0	MSTR_PAR_ERR	Set when the master asserts PERR# during a read transaction or observes PERR# asserted by target when writing data to target. The Parity Error Response bit in the command register must be enabled.
[23]	RO	1'b1	TRGT_B2B_CAP	CX25800 target is capable of fast back-to-back transactions.
[22]	RO	1'b0	Reserved	Defined as reserved in the PCI specification.
[21]	RO	1'b0	66MHZ_CAP	CX25800 is NOT designed to work at 66 MHz.
[20]	RO	1'b1	CAP_LIST	CX25800 implements a PCI capabilities list, beginning at address offset 8'h34.

[19:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[15:10]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.
[9]	RO	1'b0	MSTR_B2B_CAP	CX25800 master is not capable of fast back-to-back transactions.
[8]	RW	1'b0	SERR#_EN	SERR# driver enable. A value of 1 enables the driver. Address parity errors are reported only if this bit and Parity Error Response bit are 1.
[7]	RO	1'b0	ADR_DATA_STEP	CX25800 does not do address or data stepping.
[6]	RW	1'b0	PAR_ERR_RSP	A value of 1 enables parity error reporting.
[5]	RO	1'b0	VGA_SNP	CX25800 does not snoop VGA palette accesses.
[4]	RW	1'b0	MEM_WR_INV_EN	CX25800 does not use memory write and invalidate command, so does not need this enable.
[3]	RO	1'b0	SPCL_CYCL_EN	CX25800 does not use special cycles.
[2]	RW	1'b0	MSTR_EN	A value of 1 allows CX25800 to behave as a master.
[1]	RW	1'b0	MEM_RSP	A value of 1 allows CX25800 to respond to memory space accesses.
[0]	RO	1'b0	IO_RSP	CX25800 has no I/O address space.

Revision ID and Class Code

Register 8'h08—F3_REVID_CLASS_CFG

Register 24'h2F0308—F3_REVID_CLASS_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'h048000	CLASS_CODE	This CX25800 VIP master function is a multimedia other device.
[7:0]	RO	8'h	REV_ID	This register identifies the device revision.

Cache Line Size, Latency Timer, Header Type, BIST

Register 8'h0C—F3_LN_LAT_HDR_CFG

Register 24'h2F030C—F3_LN_LAT_HDR_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	BIST	CX25800 does not implement this BIST function.
[23:16]	RO	8'h80	HDR_TYPE	CX25800 is a multifunction PCI device.
[15:8]	RW	8'h00	LAT_TIMER	The number of PCI bus clocks for the latency timer used by the master for this function. Once the latency expires, the master initiates transaction termination as soon as GNT# is removed.
[7:0]	RW	8'h00	CACHE_LN_SZ	System software loads this with the system cache line size. This information is used by the masters using Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple.

Base Address 0

Register 8'h10—F3_BAR0_CFG

Register 24'h2F0310—F3_BAR0_MM

Bits	Type	Default	Name	Description
[31:24]	RW	8'h00	BASE_ADRS_UPR	These upper bits are written by the system software to locate the function registers in the PCI address space.
[23:0]	RO	24'h000000	BASE_ADRS_LWR	These lower bits indicate to the system software that 16 MB of nonprefetchable data are required anywhere in the 32-bit memory address space.

Subsystem Vendor and Subsystem ID

Register 8'h2C—F3_SUBSYS_ID_CFG

Register 24'h2F032C—F3_SUBSYS_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RW	16'h0000	SUBSYS_ID	This is automatically loaded at reset with the value from addresses 12'h006 (least significant byte) and 12'h007 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.
[15:0]	RW	16'h0000	SUBSYS_VNDR_ID	This is automatically loaded at reset with the value from addresses 12'h004 (least significant byte) and 12'h005 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.

Capabilities Pointer

Register 8'h34—F3_CAP_PTR_CFG

Register 24'h2F0334—F3_CAP_PTR_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'b0	Reserved	Defined as reserved in the PCI specification.
[7:0]	RO	8'h44	CAP_PTR	Dword-aligned byte address offset in configuration space to the first item in the list of capabilities.

Interrupt Line, Interrupt Pin, Minimum Grant, Maximum Latency

Register 8'h3C—F3_INT_GNT_LAT_CFG

Register 24'h2F033C—F3_INT_GNT_LAT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'hFF	MAX_LAT	Require bus access every 64 μs, in units of 250 ns. The VIP can actually tolerate up to 80 μs latency, so the maximum value for this parameter is used. Affects the setting for the latency timer.
[23:16]	RO	8'h06	MIN_GNT	Desire a minimum grant burst period of 1.5 μs, in units of 250 ns. Affects the setting for the latency timer.
[15:8]	RO	8'h01	INT_PIN	CX25800 interrupt pin is connected to INTA#.
[7:0]	RW	8'h00	INT_LINE	The interrupt line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the CX25800 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Device Control #1

Register 8'h40—F3_DEV_CNTRL1_CFG

Register 24'h2F0340—F3_DEV_CNTRL1_MM

Bits	Type	Default	Name	Description
[31:29]	RO	11'b0	Reserved	
[28]	RW	1'b1	FNC4_EN	When 1, this function is enabled. When 0, it is disabled. This bit is loaded from EEPROM automatically when PCI reset is deasserted. The R/W accessibility is for test purposes only.
[27]	RW	1'b1	FNC3_EN	Same as bit 28 above
[26]	RW	1'b1	FNC2_EN	Same as bit 28 above
[25]	RW	1'b1	FNC1_EN	Same as bit 28 above
[24]	RO	1'b1	FNC0_EN	Same as bit 28 above, except there is no write allowed. PCI function 0 cannot be disabled.
[20]	RW	1'b1	Two-wire serial interface RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[19]	RW	1'b1	GPHST_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[18]	RW	1'b1	VIP_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[17]	RW	1'b1	AUD_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[16]	RW	1'b1	VID_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.

[12]	RW	1'b1	Two-wire serial interface RDY_EN	When 1, the ready and transfer-in-progress logic for the two-wire serial interface is enabled. When 0, the logic is disabled. In this case, the two-wire serial interface XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[11]	RW	1'b1	GPHST_RDY_EN	When 1, the ready and transfer-in-progress logic for General Purpose Host is enabled. When 0, the logic is disabled. In this case, the GPHST_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[10]	RW	1'b1	VIP_RDY_EN	When 1, the ready and transfer-in-progress logic for VIP is enabled. When 0, the logic is disabled. In this case, the VIP_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[9]	RW	1'b1	AUD_RDY_EN	When 1, the ready and transfer-in-progress logic for audio is enabled. When 0, the logic is disabled. In this case, the AUD_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[8]	RW	1'b1	VID_RDY_EN	When 1, the ready and transfer-in-progress logic for video is enabled. When 0, the logic is disabled. In this case, the VID_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[6:4]	RW	3'b011	DMA_RTRY_LMT	Selects the number of retries that are allowed before the DMA arbiter switches to the other channel.
[3]	RW	1'b0	EN_VSFX	Enable VIA/SIS PCI controller compatibility mode for all functions 0, 1, 2, 3, and 4.
[0]	RW	1'b0	SVIDS_EN	A value of 1 enables writes to the Subsystem and Subsystem Vendor ID register for all functions 0, 1, 2, 3, and 4.

VPD Capability

Register 8’h44—F3_VPD_CAP_CFG

Register 24’h2F0344—F3_VPD_CAP_MM

Bits	Type	Default	Name	Description
[31]	RW	1’b0	VPD_Flag	This flag is set to a value of 1 when the device completes reading and transfer of four bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW		VPD_ADRS	Logical byte address of the VPD to be accessed.
[15:8]	RO	8’h4C	VPD_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8’h03	VPD_ID	VPD new capability data structure ID assigned by SIG.

VPD Data

Register 8’h48—F3_VPD_DATA_CFG

Register 24’h2F0348—F3_VPD_DATA_MM

Bits	Type	Default	Name	Description
[31:0]	RW*		VPD_DATA	Four bytes are always transferred between the VPD data register and the EEPROM. The LSB…MSB is transferred from/to VPD_ADRS…VPD_ADRS+3.

Power Management Capability

Register 8'h4C—F3_PWR_MAN_CAP_CFG

Register 24'h2F034C—F3_PWR_MAN_CAP_MM

Bits	Type	Default	Name	Description
[31:27]	RO	5'b00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	1'b0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	1'b0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	3'b000		Reserved
[21]	RO	1'b1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	1'b0		Reserved
[19]	RO	1'b0	PMC_PME_CLK	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	3'b010	PMC_VRSN	Function complies with version 1.1 of the PCI Power Management Specification.
[15:8]	RO	8'h00	PMC_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8'h01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

Power Management Support Registers

Register 8'h50—F3_PWR_MAN_SPRT_CFG

Register 24'h2F0350—F3_PWR_MAN_SPRT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	PWR_DATA	This field is used to report the state dependent data requested by DATA_SEL and scaled by DATA_SCALE. Optional and not supported.
[23:16]	RO	8'h00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	1'b0	PME_STATUS	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	2'b00	DATA _SCALE	This field indicates the scaling factor to be used when interpreting the value of the PWR_DATA register. Optional and not supported.
[12:9]	RO	4'h0	DATA_SEL	This field selects which data is to be reported through the PWR_DATA register. Optional and not supported.
[8]	RO	1'b0	PME_EN	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	6'h00		Reserved
[1:0]	RW	2'b00	PWR_STATE	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

Bits [15:0] are also known as the Power Management Control/Status register or PMCSR. Attempting to set PowerState to D1 or D2 results in no change of state for that 2-bit field.

5.5 PCI Configuration Registers: Function 4: Host

These registers are related to the GP Host Master function only. Since the CX25800 is a multifunction PCI device, AD[10:8] are used to indicate which function the PCI bus is addressing. This function only responds when AD[10:8] are equal to 3'b100 during a configuration type 0 transaction.

Vendor and Device ID

Register 8'h00—F4_VNDR_DEV_ID_CFG

Register 24'h2F0400—F4_VNDR_DEV_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RO	16'h8804	DEV_ID	DEV_ID = 16'h8804
[15:0]	RO	16'h14F1	VNDR_ID	VNDR_ID = 16'h14F1

Command and Status Register

Register 8'h04—F4_CMD_STAT_CFG

Register 24'h2F0404—F4_CMD_STAT_MM

Bits	Type	Default	Name	Description
[31]	RR	1'b0	PAR_ERR_DET	Set when a parity error is detected in the address or data, regardless of the Parity Error Response control bit.
[30]	RR	1'b0	SYS_ERR	Set when SERR# is asserted.
[29]	RR	1'b0	MSTR_ABRT	Set when master transaction is terminated with Master Abort.
[28]	RR	1'b0	TRGT_ABRT_RCV	Set when master transaction is terminated with Target Abort.
[27]	RO	1'b0	TRGT_ABRT_SIG	Set when target terminates transaction with Target Abort. This bit is always 0 as CX25800 does not respond with a target abort.
[26:25]	RO	2'b01	DEVSEL_TIME	Responds with medium DEVSEL# timing.
[24]	RR	1'b0	MSTR_PAR_ERR	Set when the master asserts PERR# during a read transaction or observes PERR# asserted by target when writing data to target. The Parity Error Response bit in the command register must be enabled.
[23]	RO	1'b1	TRGT_B2B_CAP	CX25800 target is capable of fast back-to-back transactions.
[22]	RO	1'b0	Reserved	Defined as reserved in the PCI specification.
[21]	RO	1'b0	66MHZ_CAP	CX25800 is NOT designed to work at 66 MHz.
[20]	RO	1'b1	CAP_LIST	CX25800 implements a PCI capabilities list, beginning at address offset 8'h34.

[19:16]	RO	4'b0	Reserved	Defined as reserved in the PCI specification.
[15:10]	RO	6'b0	Reserved	Defined as reserved in the PCI specification.
[9]	RO	1'b0	MSTR_B2B_CAP	CX25800 master is not capable of fast back-to-back transactions.
[8]	RW	1'b0	SERR#_EN	SERR# driver enable. A value of 1 enables the driver. Address parity errors are reported only if this bit and Parity Error Response bit are 1.
[7]	RO	1'b0	ADR_DATA_STEP	CX25800 does not do address or data stepping.
[6]	RW	1'b0	PAR_ERR_RSP	A value of 1 enables parity error reporting.
[5]	RO	1'b0	VGA_SNP	CX25800 does not snoop VGA palette accesses.
[4]	RW	1'b0	MEM_WR_INV_EN	CX25800 does not use memory write and invalidate command, so does not need this enable.
[3]	RO	1'b0	SPCL_CYCL_EN	CX25800 does not use special cycles.
[2]	RW	1'b0	MSTR_EN	A value of 1 allows CX25800 to behave as a master.
[1]	RW	1'b0	MEM_RSP	A value of 1 allows CX25800 to respond to memory space accesses.
[0]	RO	1'b0	IO_RSP	CX25800 has no I/O address space.

Revision ID and Class Code

Register 8'h08—F4_REVID_CLASS_CFG

Register 24'h2F0408—F4_REVID_CLASS_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24'h048000	CLASS_CODE	This CX25800 host interface function is a multimedia other device.
[7:0]	RO	8'h04	REV_ID	This register identifies the device revision.

Cache Line Size, Latency Timer, Header Type, BIST

Register 8'h0C—F4_LN_LAT_HDR_CFG

Register 24'h2F040C—F4_LN_LAT_HDR_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	BIST	CX25800 does not implement this BIST function.
[23:16]	RO	8'h80	HDR_TYPE	CX25800 is a multifunction PCI device.
[15:8]	RW	8'h00	LAT_TIMER	The number of PCI bus clocks for the latency timer used by the master for this function. Once the latency expires, the master initiates transaction termination as soon as GNT# is removed.
[7:0]	RW	8'h00	CACHE_LN_SZ	System software loads this with the system cache line size. This information is used by the masters using Memory Write and Invalidate, Memory Read Line, and Memory Read Multiple.

Base Address 0

Register 8’h10—F4_BAR0_CFG

Register 24’h2F0410—F4_BAR0_MM

Bits	Type	Default	Name	Description
[31:24]	RW	8’h00	BASE_ADRS_UPR	These upper bits are written by the system software to locate the function registers in the PCI address space.
[23:0]	RO	24’h000000	BASE_ADRS_LWR	These lower bits indicate to the system software that 16 MB of nonprefetchable data are required anywhere in the 32-bit memory address space.

Subsystem Vendor and Subsystem ID

Register 8’h2C—F4_SUBSYS_ID_CFG

Register 24’h2F042C—F4_SUBSYS_ID_MM

Bits	Type	Default	Name	Description
[31:16]	RW	16’h0000	SUBSYS_ID	This is automatically loaded at reset with the value from addresses 12’h006 (least significant byte) and 12’h007 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.
[15:0]	RW	16’h0000	SUBSYS_VNDR_ID	This is automatically loaded at reset with the value from addresses 12’h004 (least significant byte) and 12’h005 (most significant byte) in the EEPROM. It can also be written when enabled by the SVIDS_EN bit in the user-defined PCI Device Control register.

Capabilities Pointer

Register 8’h34—F4_CAP_PTR_CFG

Register 24’h2F0434—F4_CAP_PTR_MM

Bits	Type	Default	Name	Description
[31:8]	RO	24’b0	Reserved	Defined as reserved in the PCI specification.
[7:0]	RO	8’h4C	CAP_PTR	Dword-aligned byte address offset in configuration space to the first item in the list of capabilities.

Interrupt Line, Interrupt Pin, Minimum Grant, Maximum Latency

Register 8'h3C—F4_INT_GNT_LAT_CFG

Register 24'h2F043C—F4_INT_GNT_LAT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'hFF	MAX_LAT	Require bus access every 64 μs, in units of 250 ns. The host interface can actually tolerate up to 80 μs latency, so the maximum value for this parameter is used. Affects the setting for the latency timer.
[23:16]	RO	8'h06	MIN_GNT	Desire a minimum grant burst period of 1.5 μs, in units of 250 ns. Affects the setting for the latency timer.
[15:8]	RO	8'h01	INT_PIN	CX25800 interrupt pin is connected to INTA#.
[7:0]	RW	8'h00	INT_LINE	The interrupt line register communicates interrupt line routing information between the POST code and the device driver. The POST code initializes this register with a value specifying to which input (IRQ) of the system interrupt controller the CX25800 interrupt pin is connected. Device drivers can use this value to determine interrupt priority and vector information.

Device Control #1

Register 8'h40—F4_DEV_CNTRL1_CFG

Register 24'h2F0440—F4_DEV_CNTRL1_MM

Bits	Type	Default	Name	Description
[31:29]	RO	11'b0	Reserved	
[28]	RW	1'b1	FNC4_EN	When 1, this function is enabled. When 0, it is disabled. This bit is loaded from EEPROM automatically when PCI reset is deasserted. The R/W accessibility is for test purposes only.
[27]	RW	1'b1	FNC3_EN	Same as bit 28 above
[26]	RW	1'b1	FNC2_EN	Same as bit 28 above
[25]	RW	1'b1	FNC1_EN	Same as bit 28 above
[24]	RO	1'b1	FNC0_EN	Same as bit 28 above, except there is no write allowed. PCI function 0 may not be disabled.
[20]	RW	1'b1	Two-wire serial interface RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[19]	RW	1'b1	GPHST_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[18]	RW	1'b1	VIP_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[17]	RW	1'b1	AUD_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.
[16]	RW	1'b1	VID_RDY	When 1, the ready and transfer-in-progress logic has completed any previous transfers. When 0, the previous transfer has not completed, thus any attempted accesses result in a PCI retry. This bit is for test purposes, and is not accessed during normal operation.

[12]	RW	1'b1	Two-wire serial interface RDY_EN	When 1, the ready and transfer-in-progress logic for the two-wire serial interface is enabled. When 0, the logic is disabled. In this case, the two-wire serial interface XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[11]	RW	1'b1	GPHST_RDY_EN	When 1, the ready and transfer-in-progress logic for General Purpose Host is enabled. When 0, the logic is disabled. In this case, the GPHST_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[10]	RW	1'b1	VIP_RDY_EN	When 1, the ready and transfer-in-progress logic for VIP is enabled. When 0, the logic is disabled. In this case, the VIP_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[9]	RW	1'b1	AUD_RDY_EN	When 1, the ready and transfer-in-progress logic for audio is enabled. When 0, the logic is disabled. In this case, the AUD_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[8]	RW	1'b1	VID_RDY_EN	When 1, the ready and transfer-in-progress logic for video is enabled. When 0, the logic is disabled. In this case, the VID_XFER_STATUS register must be polled to ensure valid data is read and also to ensure previous transfer is complete before attempting another one.
[6:4]	RW	3'b011	DMA_RTRY_LMT	Selects the number of retries that are allowed before the DMA arbiter switches to the other channel.
[3]	RW	1'b0	EN_VSFX	Enable VIA/SIS PCI controller compatibility mode for all functions 0, 1, 2, 3, and 4.
[0]	RW	1'b0	SVIDS_EN	A value of 1 enables writes to the Subsystem and Subsystem Vendor ID register for all functions 0, 1, 2, 3, and 4.

VPD Capability

Register 8’h44—F4_VPD_CAP_CFG

Register 24’h2F0444—F4_VPD_CAP_MM

Bits	Type	Default	Name	Description
[31]	RW	1’b0	VPD_Flag	This flag is set to a value of 1 when the device completes reading and transfer of four bytes between the EEPROM and the VPD data register. The flag is reset to 0 when the device completes a 4-byte write transaction. SW initiates R or W transactions by setting this flag to 0 or 1 respectively when supplying the VPD byte address.
[30:16]	RW		VPD_ADRS	Logical byte address of the VPD to be accessed.
[15:8]	RO	8’h4C	VPD_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8’h03	VPD_ID	VPD new capability data structure ID assigned by SIG.

VPD Data

Register 8’h48—F4_VPD_DATA_CFG

Register 24’h2F0448—F4_VPD_DATA_MM

Bits	Type	Default	Name	Description
[31:0]	RW*		VPD_DATA	Four bytes are always transferred between the VPD data register and the EEPROM. The LSB…MSB is transferred from/to VPD_ADRS…VPD_ADRS+3.

Power Management Capability

Register 8'h4C—F4_PWR_MAN_CAP_CFG

Register 24'h2F044C—F4_PWR_MAN_CAP_MM

Bits	Type	Default	Name	Description
[31:27]	RO	5'b00000	PMC_PME	PME# cannot be asserted from this function.
[26]	RO	1'b0	PMC_D2	The function does not support the D2 power management state.
[25]	RO	1'b0	PMC_D1	The function does not support the D1 power management state.
[24:22]	RO	3'b000		Reserved
[21]	RO	1'b1	PMC_DSI	A value of 1 indicates that the function requires a device specific initialization sequence following transition to the D0 uninitialized state.
[20]	RO	1'b0		Reserved
[19]	RO	1'b0	PMC_PME_CLK	A value of 0 indicates that no PCI clock is required for the function to generate PME#.
[18:16]	RO	3'b010	PMC_VRSN	Function complies with version 1.1 of the PCI Power Management Specification.
[15:8]	RO	8'h00	PMC_NXT_PTR	Dword-aligned byte address offset in configuration space to the next item in the list of capabilities. A value of 0 indicates there are no more.
[7:0]	RO	8'h01	PMC_ID	PCI Power Management new capability data structure ID assigned by SIG.

Power Management Support Registers

Register 8'h50—F4_PWR_MAN_SPRT_CFG

Register 24'h2F0450—F4_PWR_MAN_SPRT_MM

Bits	Type	Default	Name	Description
[31:24]	RO	8'h00	PWR_DATA	This field is used to report the state dependent data requested by DATA_SEL and scaled by DATA_SCALE. Optional and not supported.
[23:16]	RO	8'h00	PMCSR_BSE	Reserved for bridge support extensions.
[15]	RO	1'b0	PME_STATUS	Function does not support PME# from $D3_{cold}$.
[14:13]	RO	2'b00	DATA _SCALE	This field indicates the scaling factor to be used when interpreting the value of the PWR_DATA register. Optional and not supported.
[12:9]	RO	4'h0	DATA_SEL	This field selects which data is to be reported through the PWR_DATA register. Optional and not supported.
[8]	RO	1'b0	PME_EN	Function does not support PME# from $D3_{cold}$.
[7:2]	RO	6'h00		Reserved
[1:0]	RW	2'b00	PWR_STATE	This field determines the current power state of a function and supports setting the function into a new power state. 00 = D0 01 = D1 (not supported) 10 = D2 (not supported) 11 = $D3_{hot}$

Bits [15:0] are also known as the Power Management Control/Status register or PMCSR. Attempting to set PowerState to D1 or D2 results in no change of state for that 2-bit field.

5.6 Memory Mapped Registers: Miscellaneous Control

The registers in this section are used by all functions.

NOTE: Each PCI configuration space function has a base address 0 register. Each one is assigned a different value when the system Configuration Manager allocates memory-mapped resources. The local memory-mapped registers address locations are specified as 24-bit offsets to the value loaded into the memory base address register. Internal base address is 24'hXXXXXX.

PCI DMAC FIFO Threshold

Register 24'h200000—PDMA_STHRSH

Register 24'h200010—PDMA_DTHRSH

Bits	Type	Default	Name	Description
[11:8]	RW	4'h7	PDMA_{x}ISBTHRSH	FIFO threshold for Internal System Bus (ISB) controller. Burst begins when this many FIFO entries (dwords) are available. For reliable operation and to avoid possible deadlock condition this value must be 0 < x < = 7.
[3:0]	RW	4'h7	PDMA_{x}PCITHRSH	FIFO threshold for PCI controller. Burst begins when this many FIFO entries (dwords) are available. For reliable operation and to avoid possible deadlock condition this value must be 0 < x < = 7.

PCI DMAC Target Address

Register 24'h200004—PDMA_STRGT_ADRS

Register 24'h200014—PDMA_DTRGT_ADRS

Bits	Type	Default	Name	Description
[31:0]	RW	32'b0	PDMA_{x}TRGT_ADRS	PCI target address for PCI DMA transfer.

PCI DMAC Internal Address

Register 24'h200008—PDMA_SINTL_ADRS

Register 24'h200018—PDMA_DINTL_ADRS

Bits	Type	Default	Name	Description
[31:0]	RW	32'b0	PDMA_{x}INTL_ADRS	ISB SRAM address for PCI DMA transfer.

PCI DMAC Control

Register 24'h20000C—PDMA_SCNTRL

Register 24'h20001C—PDMA_DCNTRL

Bits	Type	Default	Name	Description
[19]	RW	1'b0	PDMA_INST	Specifies the DMA is for RISC instructions (1) or data (0). This bit only exists for the destination channel (PDMA_DCNTRL).
[18:16]	RW	3'b0	PDMA_FUNC	Specifies the PCI function for which the DMA transfer is for. Used by the PCI master to use appropriate latency timer value.
[15:0]	RW	16'b0	PDMA_CNT	Byte count for PCI DMA transfer. Writing this register initiates a SRC or DST PCI DMA.

PCI Subsystem Vendor and Subsystem ID Load

Register 24'h200030—LD_SUBSYS_ID_CFG

Bits	Type	Default	Name	Description
[31:16]	WO	16'h0000	LD_SUBSYS_ID	The value written to this register is loaded into the Subsystem ID register in the PCI configuration space. It overwrites any value previously loaded.
[15:0]	WO	16'h0000	LD_SUBSYS_VNDR_ID	The value written to this register is loaded into the Subsystem Vendor ID register in the PCI configuration space. It overwrites any value previously loaded.

Device Control #2

Register 24'h200034—DEV_CNTRL2

Bits	Type	Default	Name	Description
[12]	WO	Reserved	Reserved	Reserved
[7]	WO	Reserved	Reserved	Reserved
[6]	WO	Reserved	Reserved	Reserved
[5]	WO	Reserved	RUN_RISC	A value of 1 enables the RISC controller. A value of 0 holds the RISC controller in a reset state.
[4]	WO	Reserved	Reserved	Reserved
[3:2]	WO	Reserved	Reserved	Reserved

PCI Interrupt Mask

Register 24'h200040—PCI_INT_MSK

Bits	Type	Default	Name	Description
[20:0]	RW	21'b0	PCI_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the PCI_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

PCI Interrupt Status

Register 24'h200044—PCI_INT_STAT

Bits	Type	Default	Name	Description
[20]	RR	1'b0	GPIO_INT1	Set when GPIO interrupt condition occurs on pin GPIO[23].
[19]	RR	1'b0	GPIO_INT0	Set when GPIO interrupt condition occurs on pin GPIO[22].
[18]	RR	1'b0	IR_SMP_INT	Set when 32 input samples have been collected over gpio[16] pin into GP_SAMPLE register.
[17]	RR	1'b0	Two-wire serial interface RACK	Set when a two-wire serial interface read or write operation has completed successfully. Latched on rising edge of two-wire serial interface INT. Intended for status only. Typically masked off.
[16]	RR	1'b0	Two-wire serial interface INT	Set when a two-wire serial interface read or write operation has completed.
[15]	RR	1'b0	IPB_DMA_BERR_INT	Set when the BERR signal is asserted to the ASB master during an APB DMA.
[14]	RR	1'b0	DST_DMA_BERR_INT	Set when the BERR signal is asserted to the ISB master during a DST DMA.
[13]	RR	1'b0	SRC_DMA_BERR_INT	Set when the BERR signal is asserted to the ISB master during a SRC DMA.
[12]	RR	1'b0	BRDG_BERR_INT	Set when the BERR signal is asserted to the ISB master of the PCI bridge.
[11]	RR	1'b0	RISC_WR_BERR_INT	Set when the BERR signal is asserted to the RISC controller during a write transfer.
[10]	RR	1'b0	RISC_RD_BERR_INT	Set when the BERR signal is asserted to the RISC controller during a read transfer.
[9]	RR	1'b0	DST_DMA_INT	Set when the destination DMA channel completes the current transfer.
[8]	RR	1'b0	SRC_DMA_INT	Set when the source DMA channel completes the current transfer.

[7]	RR	1'b0	TM1_INT	Set when timer TM_CNT1 reaches its limit TM_LMT1.
[4]	RO	1'b0	HST_INT	Set when a host (function 4) interrupt condition occurs. Cleared by clearing the bits of the Host Interrupt Status register.
[3]	RO	1'b0	VIP_INT	Set when a VIP (function 3) interrupt condition occurs. Cleared by clearing the bits of the VIP Interrupt Status register.
[2]	RO	1'b0	TS_INT	Set when a transport stream (function 2) interrupt condition occurs. Cleared by clearing the bits of the Transport Stream Interrupt Status register.
[1]	RO	1'b0	AUD_INT	Set when an audio (function 1) interrupt condition occurs. Cleared by clearing the bits of the Audio Interrupt Status register.
[0]	RO	1'b0	VID_INT	Set when a video (function 0) interrupt condition occurs. Cleared by clearing the bits of the Video Interrupt Status register.

PCI Interrupt Masked Status

Register 24'h200048—PCI_INT_MSTAT

Bits	Type	Default	Name	Description
[20:0]	RO	21'b0	PCI_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

PLL (Immediate Access)

Register 24'h35C008—PLL_B

Bits	Type	Default	Name	Description
[31:28]	RO	4'b0000		Reserved
[27]	RO	1'b1	PLL_LK	The value read at this bit location indicated the PLL's lock status. When high and stable, the PLL is in lock.
[26]	RW	1'b0	PLL_DDS	A value of 1 disables the ΔΣ and forces integer-only divides.
[25:24]	WO	2'b00	PLL_B_CR[1:0]	PLL_B clock rate Bus Clock Rate: 00 = 80 MHz ISB, 40 MHz IPB 01 = 100 MHz ISB, 50 MHz IPB 10,11 Reserved
[23:22]	RW	2'b10	PLL_PRE	Reference input prescale divider: 00 = divide by 2 01 = divide by 5 10 = divide by 4 11 = divide by 3
[21:16]	RW	6'h16	PLL_INT	6-bit integer divide. A value of 0 puts the PLL in a power-down state, otherwise a value >= 14 enables the PLL for normal operation as a clock synthesizer.
[15:0]	WO	16'h8E10	PLL_FRAC	16-bit fractional divide

GPIO

Register 24’h350020—GP0_IO

Register 24’h350024—GP1_IO

Register 24’h350018—GP2_IO

Register 24’h35001C—GP3_IO

Bits	Type	Default	Name	Description
[31: 26]	RO	6’h00		Reserved
[25]	RW	1’b0	GP{x}_MODE	A value of 0 enables the GPIO register interface in default mode where each set of 8 pins are controlled by a GP{x}_IO register. A value of 1 enables all 24 GPIO and/or GPOE bits to be read/written simultaneously.
[24]	RO	1’b0		Reserved
[23:16]	Wd		GP{x}_BWE	If this field is equal to 8’h00, then the whole GPIO byte register operates in normal R/W mode. If any bit is set, then the corresponding GP_OE and GP_IO bit locations are enabled for writing. If the bit write enable is not set, the corresponding GPIO bits is unaffected.
[15:8]	RW	8’h00	GP{x}_OE	A value of 1 enables corresponding GP_IO bit to be output on the GPIO pin.
[7:0]	RW*	8’h00	GP{x}_IO	Writing provides data for GPIO output pin drivers. Reading accesses data directly from input pin buffers.

NOTE:

As an example: To set GPIO 10 high on pin 117 on the CX25800, write 32’h00040404 to GP1_IO register. To set the same pin low write 32’h00040400.

The GP3_* control bits are only available in register GP3_IO. If GP3_MODE is set to 24-bit access mode, then the GPIO register interface looks like:

Register 24’h350020—GPIO

Bits	Type	Default	Name	Description
[23:0]	RW*	24’h000000	GP_IO	Writing provides data for GPIO output pin drivers. Reading accesses data directly from input pin buffers.

Register 24’h350024—GPOE

Bits	Type	Default	Name	Description
[23:0]	RW*	24’h000000	GP_OE	A value of 1 enables corresponding GP_IO bit to be output on the GPIO pin.

GPIO Interrupts Sensitivity Mode

Register 24'h350028—GPIO_ISM

Bits	Type	Default	Name	Description
[3:2]	WO	2'b00	GP_ISM_SNS	Sensitivity mode for interrupt inputs GPIO[23:22]. 0 = level-sensitive 1 = edge-sensitive
[1:0]	WO	2'b00	GP_ISM_POL	Polarity control for interrupt inputs GPIO[23:22]. 1 = active-high or posedge 0 = active-low or negedge

Timer Counters (Immediate Access)

Register 24'h35C034—TM_CNT1_LDW

Bits	Type	Default	Name	Description
[31:0]	RO	32'b0	TM_CNT1_LDW	Lower dword of timer. The timer increments every 100 ns, from 0 to the limit value, then resets to 0 and counts again. The maximum value provides for ~325 days. The upper 16 bits of the timer are captured for reading at the TM_CNT_UDW register whenever the TM_CNT_LDW register is read.

Register 24'h35C038—TM_CNT1_UDW

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	TM_CNT1_UDW	Upper 16 bits of the 48-bit timer, captured at the time the lower 32-bits were read. The timer increments every 100 ns, from 0 to the limit value, then resets to 0 and counts again. The maximum value provides for ~325 days.

Timer Limit Values (Immediate Access)

Register 24'h35C03C—TM_LMT1_LDW

Bits	Type	Default	Name	Description
[31:0]	RW	32'b0	TM_LMT1_LDW	When the current count value of the timer reaches the limit value, an interrupt TM1_INT is set. The periodic timer interrupt event rate is = 10 MHz/(TM_LMT1 + 1). If TM_LMT1 is set to 0, TM_CNT1 remains reset.

Register 24'h35C040—TM_LMT1_UDW

Bits	Type	Default	Name	Description
[31]	RW	1'b0	TM_LMT1_DIV	When 0, the timer uses PCLK/5 for its clock. When 1, the timer uses PCLK/4 for its clock.
[15:0]	RW	16'b0	TM_LMT1_UDW	When the current count value of the timer reaches the limit value, an interrupt TM1_INT is set. The periodic timer interrupt event rate is = 10 MHz/(TM_LMT1 + 1). If TM_LMT1 is set to 0, TM_CNT1 remains reset. TM_CNT1 is reset whenever TM_LMT1_UDW is written.

PINMUX_IO (Immediate Access)

Register 24'h35C044—PINMUX_IO

Bits	Type	Default	Name	Description
[7]	RW	1'b0	MPEG_PAR_EN	1 = GPIO[17:23] map to TSDAT[7:1] inputs. 0 = leave pins as GPIO.
[6:5]	RW	2'b00	VIP_MODE	2'b10 = GPIO[21:16] map to VHAD[7:2] I/O, this in combination with VHAD[1:0] allows VIP2.0 I/O mode. 2'b01 = GPIO[17:16] map to VHAD[3:2] I/O, this in combination with VHAD[1:0] allows for 4 bit VHAD bus. 2'b00 = leave pins as GPIO.
[4]	RW	1'b0	VID_SYNC_EN	1 = Video Sync signals are output on GPIO[6:0] see section 9.2.4 for detailed mapping. 0 = leave pins as GPIO.
[3]	RW	1'b0	VID8_OUT_EN	1 = map GPIO[15:8] to VIPO[9:2] VIP/ITU-656 digital video output. Data referenced to rising edge of GPCKO pin. 0 =leave pins as GPIO.
[2]	RW	1'b0	VID10_OUT_EN	1 = same mapping as in VID8_OUT_EN, with GPIO[23:22] = VIPO[1:0] for 10 bit output. 0 = leave pins as GPIO.
[1]	RW	1'b0	VID_IN_EN	1 = map GPIO[7:0] to VIPi[7:0] VIP digital video input. Data referenced to rising edge of GPCKI input pin. 0 = leave pins as GPIO.
[0]	RW	1'b0	HCS1_EN	1 = map Host chip select 1# to GPIO[23] (output mode).

AFECFG_IO (Immediate Access)

Register 24'h35C04C—AFE_CFG_IO

Bits	Type	Default	Name	Description
[31:5]	RO	27'h0000000		Reserved
[4]	RW	1'b0	DAC_PWRDN	1 = Power down audio DAC's bandgap and current references. 0 = Normal operation.
[3]	RW	1'b0	Y_PWRDN	1 = Power down Composite ADC. 0 = Normal operation.
[2]	RW	1'b0	C_PWRDN	1 = Power down Audio ADC. 0 = Normal operation.
[1]	RW	1'b0	BG_PWRDN	1 = Power down bandgap used in ADCs. 0 = Normal operation.
[0]	RW	1'b0	Reserved	Set to 0.

SRST_IO (Immediate Access)

Register 24'h35C05C—SRST_IO

Bits	Type	Default	Name	Description
[31:1]	RO	31'h0000000		Reserved
[0]	RW	1'b1	SRST_OUT	This reg bit directly controls SYS_RSTO_ pin. Intended use is for software to generate reset to external components on the same board through CX25800 pin.

Two-wire Serial Interface Direct

Register 24'h360000-24'h367FFF—Two-wire Serial Interface DIRECT

Bits	Type	Default	Name	Description
[31:0]	RW	32'b0	Two-wire serial interface DATA	A dword written to this address range causes the hardware two-wire serial interface to write the 4 bytes beginning at the two-wire serial interface chip address from address bits [14:8] and subaddress from address bits [7:0]. A dword read from this address range causes the hardware two-wire serial interface to read the 4 bytes beginning at the two-wire serial interface chip address from address bits [14:8] and subaddress from address bits [7:0].

Two-wire Serial Interface Data/Control

Register 24'h368000—Two-wire Serial Interface DATA/CONTROL

Bits	Type	Default	Name	Description
[31:24]	RW	8'b0	Two-wire serial interface DB0	First byte sent in a two-wire serial interface transaction. Typically this is the base or chip 7-bit address and the R/W bit.
[23:16]	RW	8'b0	Two-wire serial interface DB1	Second byte sent in a two-wire serial interface transaction, usually a subaddress.
[15:8]	RW	8'b0	Two-wire serial interface DB2	Third byte sent in a two-wire serial interface write transaction, usually the first data byte. After a read transaction, this byte register contains the data read from the slave.
[7]	RW	1'b0	Two-wire serial interface MODE	Two-wire serial interface mode. 0 = software. 1 = hardware.
[6]	RW	1'b0	Two-wire serial interface RATE	Two-wire serial interface timing frequency. 0 = 99.2 kHz. 1 = 396.8 kHz.
[5]	RW	1'b0	Two-wire serial interface NOSTOP	Two-wire serial interface stop mode. 0 = transmit stop at end of transaction. 1 = do not transmit stop at end of transaction. Hold SIC low.
[4]	RW	1'b0	Two-wire serial interface NOS1B	Two-wire serial interface start mode. 0 = transmit START or repeated START transaction. The R/W status from bit 24 is saved for any future one-byte transactions. 1 = enable one-byte read or write without START.
[3]	RW	1'b0	Two-wire serial interface SYNC	Two-wire serial interface synchronization. 0 = disallows the slave to insert wait states. 1 = allows the slave to insert bit-level clock wait states.
[2]	RW	1'b0	Two-wire serial interface W3BRA	Number of bytes sent and master/slave acknowledge. This bit has no meaning when two-wire serial interface NOS1B (bit 4) is high during a write transaction. 0 = write transaction of 2 bytes two-wire serial interface DB(0-1). During a 1 byte read transaction (two-wire serial interface NOS1B is high), master sends a NACK to end the reads from the slave. 1 = write transaction of 3 bytes two-wire serial interface DB(0-2). During a 1 bytes read transaction (two-wire serial interface NOS1B is high), master sends an ACK after reading the data byte.
[1]	RW	1'b1	Two-wire serial interface SIC	A value of 1 releases the SIC output, and a 0 forces the SIC output low. This bit must be set to a 1 during hardware mode. This override is for direct software control of the bus. Reading this bit provides access to the buffered SIC input pin.
[0]	RW	1'b1	Two-wire serial interface SID	A value of 1 releases the SID output, and a 0 forces the SID output low. This bit must be set to a 1 during hardware mode. This override is for direct software control of the bus. Reading this bit provides access to the buffered SID input pin.

Two-wire Serial Interface Control (Immediate Access)

Register 24'h36C004—Two-wire Serial Interface CTRL

Bits	Type	Default	Name	Description
[2]	RW	1'b0	Two-wire serial interface SLAVE_WSE	Two-wire serial interface direct mode wait state enable. This enables or disables two-wire serial interface slave wait state insertion.
[1]	RW	1'b0	Two-wire serial interface DIRECT_SPD	Two-wire serial interface Direct Mode speed. 0 = 100 kHz 1 = 400 kHz
[0]	RW	1'b0	Two-wire serial interface STOP_CTRL	Control for the two-wire serial interface following a PCI reset. This register bit is only reset on a power-on reset. 0 = No two-wire serial interface Stop issued following PCI reset. 1 = two-wire serial interface Stop issued following PCI reset.

Two-wire Serial Interface Transfer Status Register (Immediate Access)

Register 24'h36C044—Two-wire Serial Interface XFER_STATUS

Bits	Type	Default	Name	Description
[0]	RO	1'b0	XFER_IN_PROG	Two-wire serial interface transfer in progress signal. This can be used to determine when it is safe to access the two-wire serial interface registers. This register returns a value immediately, thus it does not follow the delayed read rules.

5.7 Memory Mapped Registers: Function 0: Video

NOTE: Each PCI configuration space function has a base address 0 register. Each one is assigned a different value when the system Configuration Manager allocates memory-mapped resources. The local memory-mapped registers address locations are specified as 16-bit offsets to the value loaded into the memory base address register.

Video Decoder

Device Status

Register 24'h310100

Bits	Type	Default	Name	Description
[31]	RO	20'h00000		Reserved
[30:16]	RO	15'h0000	SCHERR	Subcarrier loop filter error
[15:8]	RO	8'h00000		Reserved
[7]	RO	1'b0	NSPLAY	Special Play Status. Input vertical sync timing nonstandard 0 = in VCR special play mode 1 = Normal mode
[6]	RO	1'b0	VPRES	Video Present 0 = No video detected 1 = Video detected
[5]	RO	1'b0	HLOCK	Horizontal Lock 0 = Not locked 1 = Locked
[4]	RO	1'b0	FIELD	Field Identifier 0 = Odd field 1 = Even field
[3]	RO	1'b0	NUML	Number of lines per frame 0 = 525 1 = 625
[2]	RO	1'b0	PLL	A value of 0 indicates the PLL is out of lock. Should be checked after initializing the PLL and cleared until no longer set (up to 100 ms).
[1]	RR	1'b0	LOF	Luma ADC Over/Underflow. If a Y-A/D overflow or underflow occurs, this bit is set. It is reset by writing a 1 to this bit.
[0]	RR	1'b0	Reserved	
GENERAL NOTES: The subcarrier loop filter error is provided for subcarrier tracking status. Also, the A/D overflow bits are register type RR.				

Input Format

Register 24’310104

Bits	Type	Default	Name	Description
[31:18]	RO	14’h0000		Reserved
[17]	RW	1’b0	PESRC_SEL	0 = pixel engine input selects analog input data and clock 1 = pixel engine input selects digital input data and clock (VIP input source)
[16]	RW	1’b0	Reserved	Set to 0.
[15:14]	RW	2’b00	YADC_SEL	Video input source selection. 00 = MUX1 01 = MUX2 10 = MUX3 11 = MUX4
[13]	RW	1’b0	AGCEN	AGC Enable 0 = disable AGC 1 = enable AGC
[12]	RW	1’b0	NCAGC	AGC Gain 0 = coarse AGC gain adjust (+1) 1 = normal AGC gain (+4)
[11]	RW	1’b0	WCEN	White crush circuit monitors A/D for overflows and automatically adjusts input signal gain. 0 = Nonadaptive AGC 1 = Adaptive AGC
[10]	RW	1’b0	CAGCEN	0 = Chroma AGC disabled 1 = Chroma AGC enabled (Recommended)
[9]	RW	1’b0	CKILLEN	Enable low-color removal for all video standards. 0 = Color killer disabled 1 = Color killer enabled
[8]	RW	1’b0	SCSPD	Chroma subcarrier lock speed. 0 = Normal 1 = Fast
[7]	RW	1’b1	VERTEN	A value of 1 enables vertical sync detection in determining VPRES status.
[6:5]	RO	2’b00		Reserved
[4]	RW	1’b0	Reserved	Set to 0.
[3:0]	RW	4’b0000	FMT	Selects input video format. 0000 = Auto format detection 0001 = NTSC-M 0010 = NTSC-J 0011 = NTSC-4.43 0100 = PAL-BDGHI 0101 = PAL-M 0110 = PAL-N 0111 = PAL-Nc 1000 = PAL-60

Temporal Decimation

Register 24'h310108

Bits	Type	Default	Name	Description
[31:12]	RO	20'h00000		Reserved
[11:10]	RW	2'b00	HL_LP	Horizontal Loop Lowpass Filter Speed
[9]	RO	1'b0		Reserved
[8]	RW	1'b0	CDISE	Comparator Clamp Enable 0 = enable 1 = disable
[7]	RW	1'b0	TDFIELD	Defines whether decimation is by fields or frames. 0 = Decimate frames 1 = Decimate fields
[6]	RW	1'b0	TDALGN	Aligns start of decimation with even or odd field. 0 = Start on odd field 1 = Start on even field
[5:0]	RW	6'b000000	TEMPDEC	Number of fields or frames dropped out of 50 (625/50) or 60(525/60). This value should not exceed 60 for 60 Hz systems, or 50 for 50 Hz systems.

AGC/Burst Delays

Register 24'h31010C

Bits	Type	Default	Name	Description
[31:16]	RO	16'h0000		Reserved
[15:8]	RW	8'b6d	BGDEL	The burst gate delay for subcarrier sampling. The following equation should be used to determine the value for the register: BDELAY = (6.5 μs * video decoder core sample frequency) + 21 Example for an NTSC input signal: BDELAY = (6.5 μs x 13.50 MHz + 21 = 109 (0x6D)
[7:0]	RW	8'h63	AGCDEL	AGC gate delay for back-porch sampling. The following equation should be used to determine the value for this register: ADELAY = (6.8 μs * video decoder core sample frequency) + 15 Example for an NTSC input signal: ADELAY = (6.8 μs * 13.5 MHz) + 15 = 107 (0x6B)

Contrast and Brightness

Register 24'h310110

Bits	Type	Default	Name	Description
[31:16]	RO	16'h0000		Reserved
[15:8]	RW	8'h39	CNTRST	The decoded luminance portion of the video is multiplied by this contrast value. Values from 00 to FF are allowed.
[7:0]	RW	8'h00	BRITE	Brightness offset applied to the video. Values from 00 to FF are allowed. The 2s complement value programmed into this register is added to the decoded luminance portion of the video signal. Brightness is applied after contrast.The decoded luminance portion of the video is multiplied by this contrast value.

UV Saturation

Register 24'h310114

Bits	Type	Default	Name	Description
[31:16]	RO	16'h0000		Reserved
[15:8]	RW	8'b5A	VSAT	SAT_V gain applies to the decoded V vector of the chrominance. Values from 00 to FF are allowed.
[7:0]	RW	8'h7F	USAT	SAT_U gain applies to the decoded U vector of the chrominance. Values from 00 to FF are allowed. For ITU-R BT.656 decoding, USAT and VSAT must have equal values.

Hue

Register 24'h310118

Bits	Type	Default	Name	Description
[31:8]	RO	24'h000000		Reserved
[7:0]	RW	8'h00	HUE	HUE applies to the phase offset of the decoders internal subcarrier. Values from 00 to FF are allowed.

White Crush Up/Down

Register 24'h31011C

Bits	Type	Default	Name	Description
[31:15]]	RO	17'h00000		Reserved
[14]	RW	1'b1	WCFRAME	This bit programs the rate at which the DNCNT and UPCNT values are accumulated. 0 = Once per field 1 = Once per frame
[13:8]	RW	6'b111111	DNVAL	White crush down count value. 2s complement, a negative sign bit is assumed i.e., 3F = -1 3E = -2 … … 00 = –64
[7:6]	RW	2'b11	MAJSEL	These bits determine the majority comparison point for the white crush up function. 00 = 3/4 maximum luma 01 = 1/2 maximum luma 10 = 1/4 maximum luma 11 = Automatic
[5:0]	RW	6'b001111	UPVAL	White crush up value. The value programmed in these bits accumulates once per field or frame, in the case where the majority of the pixels in the active region of the image are below a selected value. The accumulated value determines the extent to which the AGC value must be raised in order to keep the SYNC level proportionate with the white level. The UPCNT value is assumed positive i.e., 3F = 63 3E = 62 …. … 00 = 0

Y/C Separation Notch Filter Selection and Total Pixel Count

Register 24'h310120

Bits	Type	Default	Name	Description
[31:13]	RO	19'h00000		Reserved
[12:11]	RW	2'b10	NOTCHSEL	Coefficient selection of HL notch filter 00 = use 4x Fsc optimized filter 01 = use square pixel freq. optimized filter 10 = use 13.5 MHz NTSC optimized filter 11 = use 13.5 MHz PAL optimized filter
[10:0]	RW	11'h35A	HTOTAL	Programmable total number of pixel per line

Horizontal Delay

Register 24'h310124: Even Field

Register 24'h310128: Odd Field

Bits	Type	Default	Name	Description
[31:10]	RO	21'h000000		Reserved
[9:0]	RW	10'h07E	HBLANK	This is the horizontal delay. It defines the number of scaled pixels between the falling edge of HRESET and the start of active video. Values between 1 and 1023 are allowed. For NTSC: hblank = 9.4 x F_{sample} For PAL: hblank = 10.5 x F_{sample}

Vertical Delay

Register 24'h31012C: Odd Field

Register 24'h310130: Even Field

Bits	Type	Default	Name	Description
[31:10]	RO	22'h000000		Reserved
[9:0]	RW	10'h014	VBLANK	This is the vertical delay. It defines the number of half lines between the trailing edge of VRESET and the start of active video. Values between 1 and 1023 are allowed.

Vertical Delay in ITU-R BT.656 output mode

Register 24'h310134: Odd Field

Register 24'h310138: Even Field

Bits	Type	Default	Name	Description
[31:8]	RO	24'h000000		Reserved
[7:0]	RW	8'h0C	V656BLANK	This is the vertical delay used in ITU-R BT.656 mode. It defines the number of half lines between the trailing edge of VRESET and the start of active video.

Horizontal Active

Register 24'h31013C: Even Field

Register 24'h310140: Odd Field

Bits	Type	Default	Name	Description
[31:10]	RO	22'h000000		Reserved
[9:0]	RW	10'h2D0	HACTIVE	This is the horizontal active. It defines the number of horizontal active pixels per line. Values between 1 and 1023 are allowed.

Vertical Active

Register 24’h310144: Even Field

Register 24’h310148: Odd Field

Bits	Type	Default	Name	Description
[31:10]	RO	22’h000000		Reserved
[9:0]	RW	10’h1E7	VACTIVE	This is the vertical active. It defines the number of half lines used in the vertical scaling process. Values between 1 and 1023 are allowed.

Horizontal Scaling

Register 24’h31014C: Even Field

Register 24’h310150: Odd Field

Bits	Type	Default	Name	Description
[31:16]	RO	16’h0000		Reserved
[15:0]	RW	10’h000	HSCALE	Horizontal scaling ratio.

Vertical Scaling

Register 24’h310154: Even Field

Register 24’h310158: Odd Field

Bits	Type	Default	Name	Description
[31:13]	RO	19’h00000		Reserved
[12:0]	RW	13’h0000	VSCALE	Vertical Scaling Ratio. The following equation should be used to determine the value for this register: VSF = (0x10000 –{[(scaling_ratio-1)*512}) and 0x1FFF

Horizontal/Vertical Filters Control

Register 24'h31015C: Even Field

Register 24'h310160: Odd Field

Bits	Type	Default	Name	Description
[31:23]	RO	9'h000		Reserved
[22]	RW	1'b0	P3LPFSEL	Optional LPF select in chroma path 0 = bypass 1 = enable $(1 + z^{-1})/2$ filter
[21]	RW	1'b0	P2LPFSEL	Optional LPF select in chroma path 0 = bypass 1 = enable $(1 + z^{-1})/2$ filter
[20]	RW	1'b0	P1LPFSEL	Optional LPF select in chroma path 0 = bypass 1 = enable $(1 + z^{-2})/2$ filter
[19]	RW	1'b1	CFILT	If this bit is set, this chroma filter is used when luma is not remodulated. 0 = bypass 1 = enable $(1 + 2z^{-2} + z^{-4})/4$ filter
[18]	RW	1'b0	Reserved	Set to 0.
[17]	RW	1'b0	Reserved	Set to 0.
[16]	RW	1'b0	Reserved	Set to 0.
[15:14]	RW	2'b00	Reserved	Set to 0.
[13]	RW	1'b0	LNOTCH	0 = Enable notch filter 1 = Disable (recommended for monochrome input).
[12]	RW	1'b0	LDEC	0 = Enable luma decimation filter 1 = Disable luma decimation
[11:10]	RW	2'b00	HFILT	When LDEC is a 0, used to select which horizontal low-pass filter is used. 00 = AUTO 01 = CIF 10 = QCIF 11 = ICON
[9]	RW	1'b0	PEAKEN	Enables luminance peaking filters.
[8:7]	RW	2'b00	PSEL	Selects peaking response. 00 = +2 dB at 3.58/4.43 MHz 01 = +3.5 dB at 3.58/4.43 MHz 10 = +5.0 dB at 3.58/4.43 MHz Fsc 11 = +6.0 dB at 3.58/4.43 MHz Fsc

[6:5]	RW	2'b00	COMB	Selects comb filter. 00 = Full Comb 01 = Chroma comb only 10 = reserved 11 = none
[4]	RW	1'b0	FLDALGN	Field-aligned vertical scaling 0 = Non field-aligned. Disables Interfield Interpolation 1 = Field-aligned. Enables Interfield Interpolation
[3]	RW	1'b0	VINT	VS Interlace Format 0 = Noninterlaced Vertical Scaling. Use for single field capture 1 = Interlaced Vertical Scaling. Use for capturing both fields
[2:0]	RW	3'b000	VFILT	These bits control the number of taps in the Vertical Scaling Filter. The number of taps must be chosen in conjunction with the horizontal scale factor to ensure the needed data does not overflow the internal FIFO. 000 = 2-tap interpolation only.(1) 001 = 3-tap interpolation.(2) 010 = 4-tap interpolation.(3) 011 = 5-tap interpolation.(3) 100 = 2-tap and no interpolation.(1) 101 = 3-tap and no interpolation.(2) 110 = 4-tap and no interpolation.(3) 111 = 5-tap and no interpolation.(3)

FOOTNOTES:
(1) Available at all resolutions
(2) Only available if scaling to less than 385 horizontal active pixels (CIF or smaller)
(3) Only available if scaling to less than 193 horizontal active pixels (QCIF or smaller)

Output Format and 2H Comb Control

Register 24'h310164

Bits	Type	Default	Name	Description
[31:29]	RO	3'h0		Reserved
[28]	RW	1'b1	PREVREMOD (PAL video only)	Enable previous line remodulation; must be used in conjunction with COMBALT = 1
[27]	RW	1'b1	COMBALT	3 Line/2 Line adaptive comb filter 0 = Disable (PAL) 1 = Enable (NTSC)
[26]	RW	1'b0	PAL_INV_PHASE	Used in PAL 2D comb filter mode. 0 = Normal – PAL B, D, G, H, I, and NTSC 1 = Invert – PAL M/NC
[25:16]	RW	10'h01F	COMB_RANGE	Adaptive comb filter enable threshold. If COMB_RANGE = 31, the comb filter is enabled when the pixels difference is greater than –32 and less than 31.
[15]	RW	1'b0	DISIFX	Disable IFX interpolation. 0 = Enable 1 = Disable
[14]	RW	1'b0	INVCBF	Invert sense of CBFLAG. 0 = Normal 1 = Invert
[13]	RW	1'b0	DISADAPT	Disable adaptation algorithm. 0 = Enable 1 = Disable
[12]	RW	1'b0	NARROWADAPT	Narrow adaptation algorithm. 0 = Normal 1 = Narrow
[11]	RW	1'b0	FORCE2H	Forces selection of 2H comb filtered chroma data, if 2H comb enabled with NCCOMB.
[10]	RW	1'b0	FORCEREMD	Forces remodulation of excess chroma. 0 = Adaptive remodulation 1 = Forced remodulation
[9]	RW	1'b0	NCHROMAEN	Chroma 2H comb enable. 0 = Enable 1 = Disable
[8]	RW	1'b0	NREMODEN	Remodulation enable. 0 = Enable 1 = Disable

[7:6]	RW	2'b00	YCORE	Luma Coring. The signal is truncated to 0 when level less than: 00 = 0 (no coring) 01 = 32 (5 LSBs) 10 = 64 (6 LSBs) 11 = 128 (7 LSBs)
[5:4]	RW	2'b00	CCORE	Chroma Coring. The signal is truncated to 0 when level less than: 00 = 0 (no coring) 01 = +7 (3 LSBs) 10 = +15 (4 LSBs) 11 = +31 (5 LSBs)
[3]	RW	1'b0	RANGE	Luma output range. The range must be limited when using the control codes as video timing. 0 = Normal Y:[16,253], C:[2,253] 1 = Full Range Y:[0,255], C:[2,253]
[2]	RW	1'b0	HACTEXT	HACTIVE extend.
[1]	RW	1'b0	HSFMT	Selects width of HRESET (CLKx1s) 0 = 64 1 = 32
[0]	RO	1'b0		Reserved

PLL Register

Register 24'h310168

Bits	Type	Default	Name	Description
[31:29]	RO	3'b000		Reserved
[28]	RW	1'b0	PLL_DDS	A value of 1 disables the ΔΣ and forces integer-only divides.
[27:26]	RW	2'b00	PLL_PRE	Reference input prescale divider: 00 = divide by 2 01 = divide by 5 10 = divide by 4 11 = divide by 3
[25:20]	RW	6'h0F	PLL_INT	6-bit integer divide. A value of 0 puts the PLL in a power-down state, otherwise a value > = 14 enables the PLL for normal operation as a clock synthesizer.
[19:0]	RW	20'h15F18	PLL_FRAC	20-bit fractional divide (default setting is for 28.63636 MHz xtal and 27 MHz PLL frequency)
GENERAL NOTES: The equation to derive PLL frequency is: *Desired PLL frequency = ((XTAL freq/PLL_PRE)/8) * (PLL_INT + (PLL_FRAC/2^{20}))*				

PLL Adjust Control Register

Register 24’h31016C

Bits	Type	Default	Name	Description
[31:26]	RO	6’h00		Reserved
[25]	RW	1’b1	PLL_ADJ_EN	Enable PLL adjust logic 0 = disable 1 = enable
[24:19]	RW	6’h20	PLL_MAX_OFFSET	Maximum internal PLL adjustment
[18:14]	RW	5’h07	PLL_DRIFT_TH	
[13:7]	RW	7’h63	PLL_TH2	PLL threshold
[6:0]	RW	7’h10	PLL_TH1	PLL threshold

Sample Rate Conversion Register

Register 24'h310170

Bits	Type	Default	Name	Description
[31:19]	RO	13’h0000		Reserved
[18:0]	RW	19’h21F07	SRC_REG_VAL	19bit SRC programmable value. This is a ratio of the ADC clock rate to video clock rate. (ADC sampling frequency/Video decoder core frequency) * 2^{17}

Sample Rate Conversion FIFO

Register 24’h310174

Bits	Type	Default	Name	Description
[31:22]	RO	10’h000		Reserved
[21:12]	RW	10’h3F8	SRC_UP_LMT	SRC FIFO upper limit
[11:10]	RO	2’b00		Reserved
[9:0]	RW	10’h008	SRC_LOW_LMT	SRC FIFO lower limit

Subcarrier Step Size

Register 24’h310178

Bits	Type	Default	Name	Description
[31:23]	RO	9’h000		Reserved
[22:0]	RW	23’h43E0F8	SCSTEP	Subcarrier step size SCSTEP = (8*Fsc/video decoder core clock frequency) * 2^{22}

Subcarrier Step Size for DR Line

Register 24'h31017C

Bits	Type	Default	Name	Description
[31:23]	RO	9'h000		Reserved
[22:0]	RW	23'h538e38	DRSCSTEP	Subcarrier step size for DR Line DRSCSTEP = (8*4406250/video decoder core clock frequency) * 2^{22}

Capture Control

Register 24'h310180

Bits	Type	Default	Name	Description
[31:7]	RO	25'h0000000		Reserved
[6]	RW	0	CAP_RAW_ALL	A value of 1 enables continuous raw data mode capture.
[5]	RW	0	RAW16	0 = 8xFsc 8-bit data mode (Raw Data) 1 = 4xFsc 16-bit data mode (Filtered VBI data)
[4]	RW	0	CAPTURE_VBI_ODD	A value of 1 enables VBI data to be captured into the FIFO during the odd field.
[3]	RW	0	CAPTURE_VBI_EVEN	A value of 1 enables VBI data to be captured into the FIFO during the even field.
[2]	RW	0	CAPTURE_ODD	A value of 1 enables odd capture and allows video decoder to write data to FIFOs during the odd field.
[1]	RW	0	CAPTURE_EVEN	A value of 1 enables even capture and allows video decoder to write data to FIFOs during the even field.
[0]	RW	0	FRM_DITH	0 = Dither matrix applied to consecutive lines in a field 1 = Full frame mode

Color Format/Control

Register 24'h310184

Bits	Type	Default	Name	Description
[31:15]	RO	17'h0000000		Reserved
[14]	RW	0	COLOR_EN	A value of 1 enables a color bars pattern at the input of the VDFC block.
[13]	RW	0	RGB_DED	A value of 0 enables error diffusion for RGB16/RGB15 modes. A value of 1 disables it.
[12]	RW	0	GAMMA_DIS	A value of 0 enables gamma correction removal. The inverse gamma correction factor of 2.2 or 2.8 is applied and auto-selected by the respective mode NTSC/PAL. A value of 1 disables gamma correction removal.
[11]	RW	0	WSWAP_ODD	WordSwap Odd Field. A value of 1 enables word swapping of data entering the FIFO. W2[31:16] swapped with W0[15:0].
[10]	RW	0	WSWAP_EVEN	WordSwap Even Field. A value of 1 enables word swapping of data entering the FIFO. W2[31:16] swapped with W0[15:0].
[9]	RW	0	BSWAP_ODD	ByteSwap Odd Field. A value of 1 enables byte swapping of data entering the FIFO. B3[31:24] swapped with B2[23:16] and B1[15:8] swapped with B0[7:0].
[8]	RW	0	BSWAP_EVEN	ByteSwap Even Field. A value of 1 enables byte swapping of data entering the FIFO. B3[31:24] swapped with B2[23:16] and B1[15:8] swapped with B0[7:0].
[7:4]	RW	4'b0000	COLOR_ODD	Odd Field Color Format 0000 = RGB32 0001 = RGB24 0010 = RGB16 0011 = RGB15 0100 = YUV2 4:2:2 0101 = BtYUV 4:1:1 0110 = Y8 (Gray scale) 0111 = TGB8 (Dithered) 1000 = YcrCb 4:2:2 Planar 1001 = YcrCb 4:1:1 Planar (YUV9,YUV12) 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Raw 8x Data 1111 = Reserved

[3:0]	RW	4'b0000	COLOR_EVEN	Even Field Color Format 0000 = RGB32 0001 = RGB24 0010 = RGB16 0011 = RGB15 0100 = YUV2 4:2:2 0101 = BtYUV 4:1:1 0110 = Y8 (Gray scale) 0111 = TGB8 (Dithered) 1000 = YcrCb 4:2:2 Planar 1001 = YcrCb 4:1:1 Planar 1010 = Reserved 1011 = Reserved 1100 = Reserved 1101 = Reserved 1110 = Raw 8x Data 1111 = Reserved

VBI Packet Size/Delay

Register 24'h310188

Bits	Type	Default	Name	Description
[31:29]	RO	3h0		Reserved
[28:17]	RW	12h000	FRM_SIZE	VBI Frame Size Used in both RAW all mode and VBI frame mode specifies number of bytes packed in each packet has to be QWORD boundary.
[16:11]	RW	6'h00	VBI_V_DEL	The number of CLKx1s to delay from the trailing edge of HRESET before starting VBI line capture. Used in both VBI line mode and VBI frame mode, where in VBI frame mode it has to set to a value of 2.
[10]	RW	0	EXTERN	A value of 1 extends the frame output capture region to include the 20 half lines prior to the default VACTIVE region.
[9:0]	RW	10'h000	VBI_PKT_SIZE	VBI Packet Size. The number of raw data dwords (four 8-bit samples) to capture per line while in VBI capture mode (only used in VBI line mode).

Field Capture Counter

Register 24'h310190

Bits	Type	Default	Name	Description
[31:10]	RO	22'h000000		Reserved
[9:0]	RW	10'h000	FCNTR	Counts field transitions when any CAPTURE bit is set. Any write to this register resets the content to 0.

VIP Configuration

Register 24'h310194

Bits	Type	Default	Name	Description
[31:5]	RO	27'h0000000		Reserved
[4]	RW	1'b0	VIP_DROP	Enables frame rate reduction by dropping every other frame in a progressive source, or every other field in an interlace source.
[3]	RW	1'b0	VIP_VS_INT	Enable VIP vertical scaler interface mode. Used when data from both fields is used in creating scaled image. Typically only used on interface sources when the vertical scaling ration is less than 2:1. I.E. Between full resolution and CIF resolution. Should not be used when scaling progressive scan sources.
[2]	RW	1'b0	VIP_C_SCALE	Enable Chroma scaling in vertical scaler
[1]	RW	1'b0	VIP_MODE	VIP 1.1/VIP2.0 selection 0 = VIP 1.1 1 = VIP 2.0
[0]	RW	1'b0	VIP_IN_EN	Enable VIP input port. VIP input clock must be running prior to enabling the VIP input port.

VIP Contrast and Brightness

Register 24'h310198

Bits	Type	Default	Name	Description
[31:16]	RO	16'h0000		Reserved
[15:8]	RW	8'h80	VIP_CONTRAST	The luminance portion of the VIP data is multiplied by this contrast value. Values from 00 to FF are allowed. Range is 0 to 1.992.
[7:0]	RW	8'h00	VIP_BRIGHT	Brightness offset applied to the VIP data. Values from 00 to FF are allowed. The 2s complement value programmed into this register is added to the luminance portion of the VIP data. Brightness is applied after contrast.

VIP Saturation

Register 24'h31019C

Bits	Type	Default	Name	Description
[31:8]	RO	24'h000000		Reserved
[7:0]	RW	8'h80	VIP_SAT	VIP_SAT gain applies to the VIP chroma data. Values from 00 to FF are allowed. Range is 0 to 1.992

VIP Horizontal Scaling

Register 24'h3101A0

Bits	Type	Default	Name	Description
[31:15]	RO	16'h0000		Reserved
[15:0]	RW	16'h0000	VIP_HSCALE	Horizontal Scaling Ratio

VIP Vertical Scaling

Register 24'h3101A4

Bits	Type	Default	Name	Description
[31:16]	RO	16'h0000		Reserved
[15:13]	RW	3'b000	VIP_VFILT	These bits control the number of taps in the VIP Vertical Scaling Filter. The number of taps must be chosen in conjunction with the VIP horizontal scale factor to ensure the needed data does not overflow the internal FIFO. 000 = 2-tap interpolation only(1) 001 = 3-tap interpolation(2) 010 = 4-tap interpolation(3) 011 = 5-tap interpolation(3) 100 = 2-tap and no interpolation(1) 101 = 3-tap and no interpolation(2) 110 = 4-tap and no interpolation(3) 111 = 5-tap and no interpolation(3)
[12:0]	RW	13'h000	VIP_VSCALE	Vertical Scaling Ratio

FOOTNOTES:
(1) Available at all resolution
(2) Only available if scaling to less than 385 horizontal active pixels
(3) Only available if scaling to less than 193 horizontal active pixels

VBOS Control

Register 24'h3101A8

Bits	Type	Default	Name	Description
[31:22]	RO	10'b000		Reserved
[21]	RW	1'b0	VIP_VBIT	VIP V-Bit setting 0 = normal V-bit generation 1 = new V-bit equals (V-bit and T-bit)
[20]	RW	1'b0	VIP_OPT_AL	VIP optional active line enable
[19]	RW	1'b0	CLKGT	GPCLKO gating 0 = CLKx1 or CLKx2 is inverted and gated with VALID and ACTIVE to create GPCLKO. Used in punctured clock mode. 1 = CLKx1 or CLKx2 is inverted and gated with VALID to create GPCLKO when VLDFMT = 0. Used in 656 mode.
[18]	RW	1'b1	VIP_LINE_DLY	When this bit is set, the output of the VIP control codes is delayed by one line to match the delay introduced by the comb filter.
[17]	RW	1'b0	MODE656	ITU-R-BT.656 mode 0 = disable 1 = enable
[16]	RW	1'b0	MODE10B	Pixel output mode 0 = 8 bit output 1 = 10 bit output
[15]	RW	1'b0	VBIEN	Enable VBI capture 0 = Disable VBI capture 1 = Enable VBI capture
[14]	RW	1'b0	VLDFMT	VALID format 0 = VALID indicates nonscaled pixels 1 = VALID is logical AND of nominal VALID and ACTIVE, where ACTIVE is controlled by ACTFMT. GPCLKO is inverted CLKx1 or CLKx2.
[13]	RW	1'b0	VBIFMT	VBI Output Format 0 = Pixel N on VD[15:8], Pixel N+1 on VD[7:0] 1 = Pixel N on VD[7:0], Pixel N+1 on VD[15:8]
[12]	RW	1'b0	VBIFRM	VBI Frame (raw) mode 0 = VBI frame mode disabled 1 = VBI frame mode enabled
[11]	RW	1'b1	ACTFMT	ACTIVE format 0 = ACTIVE is composite active 1 = ACTIVE is horizontal active

[10]	RW	1'b0	BSTRMEN	Enables Bytestream control code insertion 0 = No Bytestream control codes 1 = Bytestream control codes inserted
[9]	RW	1'b1	VIPEN	Enables VIP control code insertion 0 = NO VIP control codes 1 = VIP control codes inserted
[8]	RW	1'b0	NBYTE	0 = 8-bit output (GPCLKO = CLKx2) 1 = 16-bit output (GPCLKO = CLKx1)
[7:1]	RW	7'h00	VPOLE	
[0]	RO	1'b0		Reserved

AGC Back Porch/VBI/Interval Counter Control

Register 24'h310200

Bits	Type	Default	Name	Description
[31:28]	RO	4'h00		Reserved
[27]	RW	1'b0	CLAMP_VBI_EN	
[26]	RW	1'b0	AGC_VBI_EN	
[25]	RW	1'b0	BP_REF_SEL	Back Porch reference Select 0 = Selects WhiteCrush for Back Porch reference 1 = Selects BP_REF register for Back Porch reference
[24:16]	RW	9'h0E0	BP_REF	Sets desired value for Back Porch
[15:12]	RO	4'h0		Reserved
[11:0]	RW	12'h555	INTRVL_CNT_VAL	Maximum count for interval counter in min-max detect

AGC Sync Slicer

Register 24'h310204

Bits	Type	Default	Name	Description
[31:22]	RO	10'h000		Reserved
[21]	RW	1'b1	DLY_UPD_EN	
[20]	RW	1'b1	SAM_SYNC_EN	
[19]	RW	1'b1	STD_SLICE_EN	Enables standard sync slicer
[18:16]	RW	3'h4	MM_MULT	
[15:8]	RW	8'h60	BP_SAM_DLY	Back porch sample delay
[7:0]	RW	8'h1C	SYNC_SAM_DLY	Sync sample delay

AGC Sync Tip Adjust 1

Register 24'h310208

Bits	Type	Default	Name	Description
[31:29]	RO	3'b000		Reserved
[28:17]	RW	12'h1C0	TRK_MODE_THR	
[16:9]	RW	8'h00	TRK_CORE_THR	Sets coring threshold level during tracking mode
[8:7]	RW	2'b00	TRK_G_VAL	Set gain level during tracking mode 00 = x1 gain 01 = x2 gain 10 = x4 gain 11 = x8 gain
[6:0]	RW	7'h0F	TRK_SAT_VAL	Set saturation level during tracking mode

AGC Sync Tip Adjust 2

Register 24'h31020C

Bits	Type	Default	Name	Description
[31:29]	RO	3'b000		Reserved
[28:17]	RW	12'h020	ACQ_MODE_THR	
[16:9]	RW	8'h00	ACQ_CORE_THR	Sets coring threshold level during acquisition mode
[8:7]	RW	2'b01	ACQ_G_VAL	Set gain level during acquisition mode 00 = x1 gain 01 = x2 gain 10 = x4 gain 11 = x8 gain
[6:0]	RW	7'h3F	ACQ_SAT_VAL	Set saturation level during acquisition mode

AGC Sync Tip Adjust 3

Register 24'h310210

Bits	Type	Default	Name	Description
[31:29]	RO	3'b000		Reserved
[28:16]	RW	13'h1E48	LOW_STIP_TH	
[15:8]	RW	8'hE0	ACC_MIN	Accumulator
[7:0]	RW	8'h40	ACC_MAX	Accumulator

AGC Gain Adjust 1

Register 24’h310214

Bits	Type	Default	Name	Description
[31:29]	RO	3’b000		Reserved
[28:17]	RW	12’h0E0	TRK_AGC_MODE_TH	
[16:9]	RW	8’h0E	TRK_AGC_CORE_TH_VAL	Sets coring threshold level during tracking mode
[8:7]	RW	2’b00	TRK_GAIN_VAL	AGC error gain (in powers of 2) for tracking mode
[6:0]	RW	7’h07	TRK_AGC_SAT_VAL	AGC error saturation value for tracking mode

AGC Gain Adjust 2

Register 24’h310218

Bits	Type	Default	Name	Description
[31:29]	RO	3’b000		Reserved
[28:17]	RW	12’h020	ACQ_AGC_MODE_TH	
[16:9]	RW	8’h00	ACQ_AGC_CORE_TH_VAL	Sets coring threshold level during acquisition mode
[8:7]	RW	2’b10	ACQ_GAIN_VAL	AGC error gain (in powers of 2) for acquisition mode
[6:0]	RW	7’h0F	ACQ_AGC_SAT_VAL	AGC error saturation value for acquisition mode

AGC Gain Adjust 3

Register 24’h31021C

Bits	Type	Default	Name	Description
[31:24]	RO	8’h00		Reserved
[23:16]	RW	8’h28	ACC_MIN_VAL	Minimum value for AGC accumulator
[15:8]	RW	8’h38	ACC_MAX_VAL	Maximum value for AGC accumulator
[7:0]	RW	8’hC0	ACC_INC_VAL	

AGC Gain Adjust 4

Register 24’h310220

Bits	Type	Default	Name	Description
[31:24]	RO	8’h00		Reserved
[23]	RW	1’b0	INIT_6DB_VAL	0 = ON (+ 6 dB) 1 = OFF (no gain)
[22]	RW	1’b1	SLICE_REF_EN	
[21]	RW	1’b1	VGA_EN	
[20:16]	RW	5’h0A	INIT_VGA_VAL	Initial value to be loaded to the VGA counter
[15:8]	RW	8’h2C	LOW_ACC_VAL	Minimum value to be compared with digital gain accumulator output to qualify a decrement in VGA counter
[7:0]	RW	8’h34	HIGH_ACC_VAL	Maximum value to be compared with digital gain accumulator output to qualify a increment in VGA counter

IPB DMAC Current Buffer Pointer

Register 24’h300080—DMA21_PTR1

Register 24’h300084—DMA22_PTR1

Register 24’h300088—DMA23_PTR1

Register 24’h30008C—DMA24_PTR1

Bits	Type	Default	Name	Description
[23:2]	RO	22’hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2’b00		Reserved

IPB DMAC Current Table Pointer

Register 24’h3000C0—DMA21_PTR2

Register 24’h3000C4—DMA22_PTR2

Register 24’h3000C8—DMA23_PTR2

Register 24’h3000CC—DMA24_PTR2

Bits	Type	Default	Name	Description
[23:2]	RW*	22’hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2’b00		Reserved

IPB DMAC Buffer Limit

Register 24’h300100—DMA21_CNT1

Register 24’h300104—DMA22_CNT1

Register 24’h300108—DMA23_CNT1

Register 24’h30010C—DMA24_CNT1

Bits	Type	Default	Name	Description
[10:0]	RW*	11’hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

Register 24’h300140—DMA21_CNT2

Register 24’h300144—DMA22_CNT2

Register 24’h300148—DMA23_CNT2

Register 24’h30014C—DMA24_CNT2

Bits	Type	Default	Name	Description
[10:0]	RW*	11’hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.
GENERAL NOTES: Writing DMA{x}_CNT2 registers (location 24’h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.				

General Purpose Counter (Immediate Access)

Register 24’h31C020—VIDY_GP_CNT

Register 24’h31C024—VIDU_GP_CNT

Register 24’h31C028—VIDV_GP_CNT

Register 24’h31C02C—VBI_GP_CNT

Bits	Type	Default	Name	Description
[15:0]	RO	16’b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate Access)

Register 24’h31C030—VIDY_GP_CNT_CNTRL

Register 24’h31C034—VIDU_GP_CNT_CNTRL

Register 24’h31C038—VIDV_GP_CNT_CNTRL

Register 24’h31C03C—VBI_GP_CNT_CNTRL

Bits	Type	Default	Name	Description
[1:0]	WO	2’b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

IPB DMA Control (Immediate Access)

Register 24’h31C040—VID_DMA_CNTRL

Bits	Type	Default	Name	Description
[7]	RW	1’b0	VBI_ RISC _EN	VBI RISC controller enable
[6]	RW	1’b0	VIDV_ RISC _EN	Planar V RISC controller enable
[5]	RW	1’b0	VIDU_ RISC _EN	Planar U RISC controller enable
[4]	RW	1’b0	VIDY_RISC_EN	Planar Y and packed RISC controller enable
[3]	RW	1’b0	VBI_ FIFO _EN	VBI FIFO enable
[2]	RW	1’b0	VIDV_ FIFO _EN	Planar V FIFO enable
[1]	RW	1’b0	VIDU_ FIFO _EN	Planar U FIFO enable
[0]	RW	1’b0	VIDY_FIFO_EN	Planar Y and packed FIFO enable

Video Transfer Status Register (Immediate access)

Register 24’h31C044—VID_XFER_STATUS

Bits	Type	Default	Name	Description
[0]	RO	1’b0	XFER_IN_PROG	Video transfer in progress signal. This can be used to determine when it is safe to access the video registers. This register returns a value immediately; thus, it does not follow the delayed read rules.

Video Interrupt Mask

Register 24’h200050—VID_INT_MSK

Bits	Type	Default	Name	Description
[19:0]	RW	20’b0	VID_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the VID_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

Video Interrupt Status

Register 24'h200054—VID_INT_STAT

Bits	Type	Default	Name	Description
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/ target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[15]	RR	1'b0	VBI_SYNC	Set when number of lines or bytes do not match the VBI RISC program expectations.
[14]	RR	1'b0	V_SYNC	Set when number of lines or bytes do not match the V video RISC program expectations.
[13]	RR	1'b0	U_SYNC	Set when number of lines or bytes do not match the U video RISC program expectations.
[12]	RR	1'b0	Y_SYNC	Set when number of lines or bytes do not match the Y video RISC program expectations.
[11]	RR	1'b0	VBIF_OF	Set when VBI FIFO overflow condition is being handled.
[10]	RR	1'b0	VF_OF	Set when V video FIFO overflow condition is being handled.
[9]	RR	1'b0	UF_OF	Set when U video FIFO overflow condition is being handled.
[8]	RR	1'b0	YF_OF	Set when Y video FIFO overflow condition is being handled.
[7]	RR	1'b0	VBI_RISCI2	Set when the IRQ2 bit in a VBI RISC instruction is set.
[6]	RR	1'b0	V_RISCI2	Set when the IRQ2 bit in a V video RISC instruction is set.
[5]	RR	1'b0	U_RISCI2	Set when the IRQ2 bit in a U video RISC instruction is set.
[4]	RR	1'b0	Y_RISCI2	Set when the IRQ2 bit in a Y video RISC instruction is set.
[3]	RR	1'b0	VBI_RISCI1	Set when the IRQ1 bit in a VBI RISC instruction is set.
[2]	RR	1'b0	V_RISCI1	Set when the IRQ1 bit in a V video RISC instruction is set.
[1]	RR	1'b0	U_RISCI1	Set when the IRQ1 bit in a U video RISC instruction is set.
[0]	RR	1'b0	Y_RISCI1	Set when the IRQ1 bit in a Y video RISC instruction is set.

Video Interrupt Masked Status

Register 24'h200058—VID_INT_MSTAT

Bits	Type	Default	Name	Description
[19:0]	RO	20'b0	VID_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

Video Interrupt Set Status

Register —

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	VID_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

5.8 Memory Mapped Registers: Function 1: Audio

AUD_CTL

Register 24'h32058C

Bits	Type	Default	Name	Description
[5:0]	RW*	6'h00	SOFT_RESET	Enable software reset of everything other than the programmable registers. Used to keep the audio subsection in a known state until all programming is complete.
[6]	RW*	1'b0	Reserved	Reserved
[8:7]	RW*	2'h0	Reserved	Reserved
[9]	RW*	1'b0	Reserved	Reserved
[10]	RW*	1'b0	Reserved	Reserved
[11]	RW*	1'b0	Reserved	Reserved
[12]	RW*	1'b0	DAC_ENABLE	DAC enable bit
[13]	RW*	1'b0	I^2SOUT_ENABLE	I^2S output enable bit
[14]	RW*	1'b0	I^2S_STR2DAC	I^2S input direct to DAC enable bit
[15]	RW*	1'b0	I^2SIN_ENABLE	I^2S input enable

VOL_CTL

Register 24'h320594

Bits	Type	Default	Name	Description
[5:0]	RW*	8'h00	VOLUME	Volume control in dB steps. 0 to –63 dB
[6]	RW*	1'b0	SRC_MUTE_EN	Source mute enable
[7]	RW*	1'b0	I^2S_MUTE_EN	I^2S mute enable
[8]	RW*	1'b0	DAC_MUTE_EN	DAC mute enable
[15:9]	RW*	7'h00		Reserved

BAL_CTL

Register 24'h320598

Bits	Type	Default	Name	Description
[5:0]	RW*	8'h00	BAL_LEVEL	Attenuation to be provided to the selected channel in dB. Range is 0 to –63 dB.
[6]	RW*	1'b0	BAL_LEFT	Select left channel for balance control if 1, select right channel if 0
[15:7]	RO*	7'h00		Reserved

I2SINPUT

Register 24'h320120

Bits	Type	Default	Name	Description
[0]	RW*	1'b0	NSlaveMaster	0 = Chip is slave 1 = Chip is master
[1]	RW*	1'b0	NPhilipsSony	0 = Conform to Philips specification 1 = Conform to Sony specification
[2]	RW*	1'b0	DisableAutoBaud	0 = Autobaud 1 = Disable autobaud
[15:3]	RO	13'h0000		Reserved

I2SINPUTSTATUS

Register 24'h320000

Bits	Type	Default	Name	Description
[5:0]	RO	6'h000	Status	0 = 0 kHz 1 = 48 kHz 2 = 96 kHz 3 = 144 kHz 4 = 192 kHz 5 = 240 kHz (not supported) 6 = 288 kHz (not supported) > 6 = > 288 kHz (not supported)
[15:6]	RO	9'h000		Reserved

2SOUTPUT

Register 24'h320128

Bits	Type	Default	Name	Description
[0]	RW*	1'b0	NPhilipsSony	0 = Conform to Philips specification 1 = Conform to Sony specification
[1]	RW*	1'b0	Mute	Holds SCK, WS, and SD outputs
[15:2]	RW*	14'h0000		Reserved

IPB DMAC Current Buffer Pointer

Register 24’h300090—DMA25_PTR1

Register 24’h300094—DMA26_PTR1

Register 24’h300098—DMA27_PTR1

Bits	Type	Default	Name	Description
[23:2]	RO	22’hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2’b00		Reserved

IPB DMAC Current Table Pointer

Register 24’h3000D0—DMA25_PTR2

Register 24’h3000D4—DMA26_PTR2

Register 24’h3000D8—DMA27_PTR2

Bits	Type	Default	Name	Description
[23:2]	RW*	22’hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2’b00		Reserved

IPB DMAC Buffer Limit

Register 24’h300110—DMA25_CNT1

Register 24’h300114—DMA26_CNT1

Register 24’h300118—DMA27_CNT1

Bits	Type	Default	Name	Description
[10:0]	RW*	11’hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

Register 24’h300150—DMA25_CNT2

Register 24’h300154—DMA26_CNT2

Register 24’h300158—DMA27_CNT2

Bits	Type	Default	Name	Description
[10:0]	RW*	11’hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.
GENERAL NOTES: Writing DMA{x}_CNT2 registers (location 24’h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.				

General Purpose Counter (Immediate Access)

Register 24'h32C020—AUDD_GP_CNT

Register 24'h32C024—AUDU_GP_CNT

Register 24'h32C028—AUDR_GP_CNT

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate Access)

Register 24'h32C030—AUDD_GP_CNT_CNTRL

Register 24'h32C034—AUDU_GP_CNT_CNTRL

Register 24'h32C038—AUDR_GP_CNT_CNTRL

Bits	Type	Default	Name	Description
[1:0]	WO	2'b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

IPB DMA Control (Immediate Access)

Register 24'h32C040—AUD_DMA_CNTRL

Bits	Type	Default	Name	Description
[6]	RW	1'b0	AUDR_ RISC _EN	Audio RDS RISC enable.
[5]	RW	1'b0	AUDU_ RISC _EN	Audio upstream RISC enable.
[4]	RW	1'b0	AUDD_ RISC _EN	Audio downstream RISC enable.
[2]	RW	1'b0	AUDR_ FIFO _EN	Audio RDS FIFO enable.
[1]	RW	1'b0	AUDU_ FIFO _EN	Audio upstream FIFO enable.
[0]	RW	1'b0	AUDD_ FIFO _EN	Audio downstream FIFO enable.

Audio Transfer Status Register (Immediate Access)

Register 24'h32C044—AUD_XFER_STATUS

Bits	Type	Default	Name	Description
[0]	RO	1'b0	XFER_IN_PROG	Audio transfer in progress signal. This may be used to determine when it is safe to access the audio registers. This register returns a value immediately, thus it does not follow the delayed read rules.

Line Length

Register 24'h32C048—AUDD_LNGTH

Register 24'h32C04C—AUDR_LNGTH

Bits	Type	Default	Name	Description
[11:0]	RW	12'b0	AUD{x}_LNGTH	Audio downstream line length in bytes.

Audio Interrupt Mask

Register 24'h200060—AUD_INT_MSK

Bits	Type	Default	Name	Description
[21:0]	RW	22'b0	AUD_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the AUD_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

Audio Interrupt Status

Register 24'h200064—AUD_INT_STAT

Bits	Type	Default	Name	Description
[21]	RR	1'b0	MCHG_IRQ	Mode change, set when operational mode changes without software intervention.
[20]	RR	1'b0	Reserved	Reserved
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/ target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[14]	RR	1'b0	RDS_DN_SYNC	Set when number of lines or bytes do not match the RDS downstream audio RISC program expectations.
[13]	RR	1'b0	UP_SYNC	Set when number of lines or bytes do not match the upstream audio RISC program expectations.
[12]	RR	1'b0	DN_SYNC	Set when number of lines or bytes do not match the downstream audio RISC program expectations.
[10]	RR	1'b0	RDS_DNF_OF	Set when downstream RDS audio FIFO overflow condition is being handled.

[9]	RR	1'b0	UPF_UF	Set when upstream audio FIFO underflow condition is being handled.
[8]	RR	1'b0	DNF_OF	Set when downstream audio FIFO overflow condition is being handled.
[6]	RR	1'b0	RDS_DN_RISCI2	Set when the IRQ2 bit in a RDS downstream audio RISC instruction is set.
[5]	RR	1'b0	UP_RISCI2	Set when the IRQ2 bit in an upstream audio RISC instruction is set.
[4]	RR	1'b0	DN_RISCI2	Set when the IRQ2 bit in a downstream audio RISC instruction is set.
[2]	RR	1'b0	RDS_DN_RISCI1	Set when the IRQ1 bit in a RDS downstream audio RISC instruction is set.
[1]	RR	1'b0	UP_RISCI1	Set when the IRQ1 bit in an upstream audio RISC instruction is set.
[0]	RR	1'b0	DN_RISCI1	Set when the IRQ1 bit in a downstream audio RISC instruction is set.

Audio Interrupt Masked Status

Register 24'h200068—AUD_INT_MSTAT

Bits	Type	Default	Name	Description
[21:0]	RO	22'b0	AUD_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

Audio Interrupt Set Status

Register 24'h20006C—AUD_INT_SSTAT

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	AUD_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

5.9 Memory Mapped Registers: Function 2: MPEG TS

IPB DMAC Current Buffer Pointer

Register 24'h30009C—DMA28_PTR1

Bits	Type	Default	Name	Description
[23:2]	RO	22'hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Current Table Pointer

Register 24'h3000DC—DMA28_PTR2

Bits	Type	Default	Name	Description
[23:2]	RW*	22'hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Buffer Limit

Register 24'h30011C—DMA28_CNT1

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

Register 24'h30015C—DMA28_CNT2

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.
GENERAL NOTES: Writing DMA{x}_CNT2 registers (location 24'h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.				

General Purpose Counter (Immediate Access)

Register 24'h33C020—TS_GP_CNT

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate Access)

Register 24'h33C030—TS_GP_CNT_CNTRL

Bits	Type	Default	Name	Description
[1:0]	WO	2'b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

IPB DMA Control (Immediate Access)

Register 24'h33C040—TS_DMA_CNTRL

Bits	Type	Default	Name	Description
[4]	RW	1'b0	TS_RISC_EN	Transport stream RISC controller enable.
[0]	RW	1'b0	TS_FIFO_EN	Transport stream FIFO enable.

Transport Stream Transfer Status Register (Immediate Access)

Register 24'h33C044—TS_XFER_STATUS

Bits	Type	Default	Name	Description
[0]	RO	1'b0	XFER_IN_PROG	Transport stream transfer in progress signal. This can be used to determine when it is safe to access the transport stream registers. This register returns a value immediately, thus it does not follow the delayed read rules.

Line Length (Immediate Access)

Register 24'h33C048—TS_LNGTH

Bits	Type	Default	Name	Description
[11:0]	RW	12'b0	TS_LNGTH	Transport stream line length in bytes.

HW SOP Control (Immediate Access)

Register 24'h33C04C—HW_SOP_CONTROL

Bits	Type	Default	Name	Description
[23:16]	RW	8'd47	IPB_STRT_BYTE	Byte start pattern that is searched for in the MPEG transport stream that signals start of transport stream. This is issued every MPEG packet.
[15:4]	RW	12'd188	IPB_PKT_LNGTH	Used to sync/mark detect SOP
[3:0]	RW	4'b0000	IPB_STRT_FLTR_CNT	Defines the number of IPB_strt_bytes that need to be detected before the MPEG fec interface is declared as being in sync.

TS General Control (Immediate Access)

Register 24'h33C050—TS_GEN_CONTROL

Bits	Type	Default	Name	Description
[7]	WO	1'b0	IPB_STAT_CLR	Active-High reset for stat registers.
[6]	WO	1'b0	IPB_SW_RST	Active-High Software reset.
[5]	RW	1'b0	IPB_ERR_ACK	Determines whether the interface is in an error ack mode. This is only valid while IPB_PUNC_CLK is active.
[4]	RW	1'b0	IPB_BIT_RVRS	This reverses each byte-wide input one byte at a time.
[3]	RW	1'b1	IPB_SMODE	Input Mode Select. 0 = Parallel Mode 1 = Serial Mode
[2]	RW	1'b0	IPB_PUNC_CLK	Determines whether the TS interface is operating in punctured clock mode.
[1]	RW	1'b0	IPB_MCLK_POL	Polarity of MPEG generated MCLK. Default means TS inputs are negedge driven. When asserted high TS inputs are negedge sampled and assumed posedge driven.
[0]	RO	1'b0	MPEG_IN_SYNC	Active-high synchronization indicator for MPEG.

TS Bad Packet Status (Immediate Access)

Register 24'h33C054—TS_BD_PKT_STATUS

Bits	Type	Default	Name	Description
[12]	RW	1'b0	IPB_BAD_PKT_CHK	Enables bad pkt status and MPEG_BAD_PKT interrupt
[11:0]	RO	12'h000	MPG_BAD_PKT_STAT	Bad pkt counter status. When enabled, counter output is incremented every time a packet number of bytes received is less than or greater than the expected programmed number of bytes.

TS SOP Status (Immediate Access)

Register 24'h33C058—TS_SOP_STATUS

Bits	Type	Default	Name	Description
[16]	RW	1'b0	IPB_TSSOP_POL	Polarity select 0 = Active High (default) 1 = Active Low
[15:14]	RW	2'b00	IPB_SOP_SEL	SOP Format. 00 = detects rising edge of TSSOP input 01 = detects rising edge of TSVALERR input 10 = detects rise and fall edge of TSSOP input 11 = detects start byte in data stream
[13]	RW	1'b0	IPB_SOP_BYTEWIDE	SOP width select. Byte wide is only an option in serial mode. 0 = Bit width 1 = Byte width
[12]	RW	1'b0	IPB_SOP_SYNC_CHK	Enables bad sop status and mpeg_bad_pkt interrupt
[11:0]	RO	12'h000	MPG_BAD_SOP_STAT	Bad SOP counter status. When enabled, counter output is incremented every time there is a SOP mis-compare. Counter status is updated at the falling edge of TS_BAD_PKT interrupt, generated by the internal mpeg_ts.

TS Fifo Overflow Status (Immediate Access)

Register 24'h33C05C—TS_FIFO_OVFL_STAT

Bits	Type	Default	Name	Description
[12]	RW	1'b0	IPB_FIFO_OVFL_CHK	Enables FIFO overflow status and mpeg_bad_pkt
[11:0]	RO	12'h000	MPG_FIFO_OVFL_STAT	When enabled the counter output is incremented every time the MPEG TS FIFO overflows.

TS Valid Miscellaneous (Immediate Access)

Register 24'h33C060—TS_VLD_MISC

Bits	Type	Default	Name	Description
[13]	RW	1'b0	IPB_TSVALERR_POL	Control for polarity of tsvalerr input. 0 = Active-High (Default) 1 = Active-Low
[12]	RW	1'b0	IPB_VAL_SEL	Selects whether tsvalerr is active. 0 = selects the external tsvalerr (default) 1 = internally generated valid
[11:0]	RW	12'h000	IPB_VAL_LNGTH	Programmable valid length. Used when mode requires TS to be terminated after a count versus the input valid (tsvalerr)

Transport Stream Interrupt Mask

Register 24'h200070—TS_INT_MSK

Bits	Type	Default	Name	Description
[20:0]	RW	21'b0	TS_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the TS_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

Transport Stream Interrupt Status

Register 24'h200074—TS_INT_STAT

Bits	Type	Default	Name	Description
[20]	RR	1'b0	TS_BAD_PCKT	Set when the MPEG transport stream interface detects an error (either of the three status check bits are set and the appropriate error condition is detected).
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/ target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[12]	RR	1'b0	TS_SYNC	Set when number of lines or bytes do not match the transport stream RISC program expectations.
[8]	RR	1'b0	TSF_OF	Set when transport stream FIFO overflow condition is being handled.
[4]	RR	1'b0	TS_RISCI2	Set when the IRQ2 bit in a transport stream RISC instruction is set.
[0]	RR	1'b0	TS_RISCI1	Set when the IRQ1 bit in a transport stream RISC instruction is set.

Transport Stream Interrupt Masked Status

Register 24'h200078—TS_INT_MSTAT

Bits	Type	Default	Name	Description
[20:0]	RO	21'b0	TS_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

Transport Stream Interrupt Set Status

Register 24'h20007C—TS_INT_SSTAT

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	TS_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

5.10 Memory Mapped Registers: Function 3: VIP

IPB DMAC Current Buffer Pointer

Register 24'h3000A0—DMA29_PTR1

Register 24'h3000A4—DMA30_PTR1

Bits	Type	Default	Name	Description
[23:2]	RO	22'hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Current Table Pointer

Register 24'h3000E0—DMA29_PTR2

Register 24'h3000E4—DMA30_PTR2

Bits	Type	Default	Name	Description
[23:2]	RW*	22'hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Buffer Limit

Register 24'h300120—DMA29_CNT1

Register 24'h300124—DMA30_CNT1

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

Register 24'h300160—DMA29_CNT2

Register 24'h300164—DMA30_CNT2

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.
GENERAL NOTES: Writing DMA{x}_CNT2 registers (location 24'h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.				

General Purpose Counter (Immediate Access)

Register 24’h34C020—VIPD_GP_CNT

Register 24’h34C024—VIPU_GP_CNT

Bits	Type	Default	Name	Description
[15:0]	RO	16’b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate Access)

Register 24’h34C030—VIPD_GP_CNT_CNTRL

Register 24’h34C034—VIPU_GP_CNT_CNTRL

Bits	Type	Default	Name	Description
[1:0]	WO	2’b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

VIP Streaming Enable (Immediate Access)

Register 24’h34C040—VIP_STREAM_EN

Bits	Type	Default	Name	Description
[5]	RW	1’b0	VIPU_RISC_EN	RISC Controller enable for the VIP interface upstream DMA channel.
[4]	RW	1’b0	VIPD_RISC_EN	RISC Controller enable for the VIP interface downstream DMA channel
[1]	RW	1’b0	VIPU_FIFO_EN	Enable for pulling data out of the VIP upstream DMA FIFO or cluster descriptor table.
[0]	RW	1’b0	VIPD_FIFO_EN	Enable for fetching downstream data from the external source.

VIP Transfer Status Register (Immediate Access)

Register 24'h34C044—XFER_STATUS

Bits	Type	Default	Name	Description
[4]	RO	1'b0	Timeout_ch1	This register should be read following a VIP time-out interrupt to determine if the register R/W channel has timed out.
[3]	RO	1'b0	Timeout_ch2	This register should be read following a VIP time-out interrupt to determine if the downstream DMA channel has timed out.
[2]	RO	1'b0	Timeout_ch3	This register should be read following a VIP time-out interrupt to determine if the upstream DMA channel has timed out.
[1]	RO	1'bx	VIP_slave_detect	This register is set to a logic 1 when the VIP detects a presence of a VIP compliant slave device. This value is set by the slave a result of the slave pulling-down HAD[0] during reset.
[0]	RO	1'b0	Xfer_in_progress	VIP transfer in progress signal. This may be used to determine when it is safe to access the host. This register returns a value immediately, thus it does not follow the delayed read rules.

VIP Configuration

Register 24'h340048—VIP_CFG

Bits	Type	Default	Name	Description
[11:8]	RW	4'b1111	VIP Timeout_length	VIP time-out length
[7:6]	RW	2'b00	Peripheral #1 config	2'b00 = 1x configuration (2-bit) 2'b01 = 2x configuration (4-bit) 2'b10 = reserved 2'b11 = 4x configuration (8-bit)
[5:4]	RW	2'b00	Peripheral #2 config	See channel #1 above.
[3:2]	RW	2'b00	Peripheral #3 config	See channel #1 above.
[1:0]	RW	2'b00	Peripheral #4 config	See channel #1 above.

VIP Upstream DMA Control Register #1

Register 24'h34004C—VIPU_DMA_CTRL1

Bits	Type	Default	Name	Description
[23:0]	RW	24'hxxxxxx	VIPU_DST_ADDR	VIP upstream IPB DMA Destination address.

VIP Downstream DMA Control Register #2

Register 24'h340050—VIPD_DMA_CTRL2

Bits	Type	Default	Name	Description
[23:0]	RW	24'hxxxxxx	VIPD_SRC_ADDR	VIP downstream IPB DMA source address.

VIP Downstream DMA Control Register #3

Register 24'h340054—VIPD_DMA_CTRL3

Bits	Type	Default	Name	Description
[11:0]	RW	12'hxxx	VIP_LNGTH	VIP downstream transfer count in bytes.

VIP Downstream DMA Control Register #4

Register 24'h340058—VIP_BURST_LENGTH

Bits	Type	Default	Name	Description
[15:8]	RW	8'hFF	VIPU_BURST_LNGTH	VIP Maximum Upstream burst length in terms of VIP data cycles. This value entered here should depend upon VIP mode (1x, 2x,4x) 1x = 1byte/data cycle, 2x = 2 bytes/data cycle…
[7:0]	RW	8'hFF	VIPD_BURST_LNGTH	Maximum burst length for Downstream transfers.

VIP Interrupt Control Register

Register 24'h34C05C—VIP_INTR_CTRL

Bits	Type	Default	Name	Description
[1]	RW	1'b0	VIP_intr_type	Level or Edge sensitive interrupt. 0 = level sensitive 1 = edge sensitive
[0]	RW	1'b0	VIP_intr_polarity	Interrupt polarity. 0 = active low 1 = active high

VIP Terminate Register

Register 24'h340060—VIP_XFER_TERMINATE

Bits	Type	Default	Name	Description
[14:5]	RW	10'h3FF	P1_retry_limit	This caps off how many retries are attempted to a VIP slave on a target read or write.
[4]	WO	1'b1	VIP_system_rst	Software controllable reset for the entire VIP subsystem (VIP Clock Domain Only). Writing a 0 causes a reset pulse to the VIP block.
[3]	WO	1'b1	VIP_core_rst	Software controllable reset for the VIP core. Writing a 0 causes a reset pulse to the ISI block.
[2]	WO	1'b0	Terminate_ch1	Writing a 1 to this register causes the VIP transfer state machine for the register R/W channel to be reset.
[1]	WO	1'b0	Terminate_ch2	Writing a 1 to this register causes the VIP transfer state machine for the downstream DMA channel to be reset.
[0]	WO	1'b0	Terminate_ch3	Writing a 1 to this register causes the VIP transfer state machine for the upstream DMA channel to be reset.

VIP Interrupt Mask

Register 24'h200080—VIP_INT_MSK

Bits	Type	Default	Name	Description
[21:0]	RW	22'b0	VIP_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the VIP_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

VIP Interrupt Status

Register 24'h200084—VIP_INT_STAT

Bits	Type	Default	Name	Description
[21]	RR	1'b0	VIP_TM_OUT	Set when a time-out occurs during a VIP transfer.
[20]	RR	1'b0	VIP_EXT	Set when the VIP external interrupt signal is asserted.
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/ target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[13]	RR	1'b0	UP_SYNC	Set when number of lines or bytes do not match the upstream VIP RISC program expectations.
[12]	RR	1'b0	DN_SYNC	Set when number of lines or bytes do not match the downstream VIP RISC program expectations.
[9]	RR	1'b0	UPF_UF	Set when upstream VIP FIFO underflow condition is being handled.
[8]	RR	1'b0	DNF_OF	Set when downstream VIP FIFO overflow condition is being handled.
[5]	RR	1'b0	UP_RISCI2	Set when the IRQ2 bit in a upstream VIP RISC instruction is set.
[4]	RR	1'b0	DN_RISCI2	Set when the IRQ2 bit in a downstream VIP RISC instruction is set.
[1]	RR	1'b0	UP_RISCI1	Set when the IRQ1 bit in a upstream VIP RISC instruction is set.
[0]	RR	1'b0	DN_RISCI1	Set when the IRQ1 bit in a downstream VIP RISC instruction is set.

VIP Interrupt Masked Status

Register 24'h200088—VIP_INT_MSTAT

Bits	Type	Default	Name	Description
[21:0]	RO	22'b0	VIP_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

VIP Interrupt Set Status

Register 24'h20008C—VIP_INT_SSTAT

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	VIP_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

5.11 Memory Mapped Registers: Function 4: Host

IPB DMAC Current Buffer Pointer

Register 24'h3000A8—DMA31_PTR1

Register 24'h3000AC—DMA32_PTR1

Bits	Type	Default	Name	Description
[23:2]	RO	22'hxxxxxx	DMA{x}_PTR1	Current DMA qword address pointer. Points to next qword transfer location within source or destination buffer. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Current Table Pointer

Register 24'h3000E8—DMA31_PTR2

Register 24'h3000EC—DMA32_PTR2

Bits	Type	Default	Name	Description
[23:2]	RW*	22'hxxxxxx	DMA{x}_PTR2	Current DMA CDT address pointer. Points to current CDT entry. Always dword-aligned.
[1:0]	RO	2'b00		Reserved

IPB DMAC Buffer Limit

Register 24'h300128—DMA31_CNT1

Register 24'h30012C—DMA32_CNT1

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT1	Initialize to DMA buffer size in number of qwords. Increments during DMA data transfers and reloads when next CDT pointer is fetched.

IPB DMAC Table Size

Register 24'h300168—DMA31_CNT2

Register 24'h30016C—DMA32_CNT2

Bits	Type	Default	Name	Description
[10:0]	RW*	11'hxxx	DMA{x}_CNT2	Initialize to DMA CDT size in number of qwords.
GENERAL NOTES: Writing DMA{x}_CNT2 registers (location 24'h300140_14C) causes the hardware to begin using the CDT information. It is imperative to perform this step only after initialization of the Cluster Description Table, Cluster Buffer Size, and CDT location.				

General Purpose Counter (Immediate Access)

Register 24'h38C020—HSTD_GP_CNT

Register 24'h38C024—HSTU_GP_CNT

Bits	Type	Default	Name	Description
[15:0]	RO	16'b0	{x}_GP_CNT	General purpose counter used by RISC program.

General Purpose Counter Control (Immediate Access)

Register 24'h38C030—HSTD_GP_CNT_CNTRL

Register 24'h38C034—HSTU_GP_CNT_CNTRL

Bits	Type	Default	Name	Description
[1:0]	WO	2'b00	{x}_GP_CNT_CNTRL	General purpose counter control used by RISC program: 00 = no change 01 = increment 10 = reserved 11 = reset to 0

Host Interface Streaming Enable (Immediate Access)

Register 24'h38C040—HST_STREAM_EN

Bits	Type	Default	Name	Description
[5]	RW	1'b0	HSTU_RISC_EN	RISC Controller enable for the host interface upstream DMA channel.
[4]	RW	1'b0	HSTD_RISC_EN	RISC Controller enable for the host interface downstream DMA channel
[1]	RW	1'b0	HSTU_FIFO_EN	Enable for pulling data out of the host upstream DMA FIFO or cluster descriptor table.
[0]	RW	1'b0	HSTD_FIFO_EN	Enable for fetching downstream data from the external source.

Host Transfer Status Register (Immediate Access)

Register 24'h38C044—XFER_STATUS

Bits	Type	Default	Name	Description
[0]	RO	1'b0	Xfer_in_progress	Host transfer in progress signal. This may be used to determine when it is safe to access the host. This register returns a value immediately, thus it does not follow the delayed read rules.

Host Upstream DMA Control Register #1

Register 24'h380048—HSTU_DMA_CTRL1

Bits	Type	Default	Name	Description
[25]	RW	1'b0	UP_FIFO_HK_EN	Host upstream FIFO handshake enable. This enables the CX25800 to monitor the External_fifo_busy bit and act accordingly.
[24]	RW	1'b0	HSTU_AINC_EN	Host upstream address auto-increment enable. Used to DMA data to sequential addresses within the slave device. Not to be used when the destination is a FIFO.
[23:0]	RW	24'hxxxxxx	HSTU_DST_ADDR	HST upstream IPB DMA Destination address. If auto increment is enabled then the value loaded into this register should be the starting address.

Host Downstream DMA Control Register #1

Register 24'h38004C—HSTD_DMA_CTRL1

Bits	Type	Default	Name	Description
[25]	RW	1'b0	DN_FIFO_HK_EN	Host downstream FIFO handshake enable. This enables the CX25800 to monitor the External_fifo_busy bit and act accordingly.
[24]	RW	1'b0	HSTD_AINC_EN	Host downstream address auto-increment enable. Used to DMA data to sequential addresses within the slave device. Not to be used when the destination is a FIFO.
[23:0]	RW	24'hxxxxxx	HSTD_SRC_ADDR	HOST downstream IPB DMA source address. If auto increment is enabled then the value loaded into this register should be the starting address.

Host Downstream DMA Control Register #2

Register 24'h380050—HSTD_DMA_CTRL2

Bits	Type	Default	Name	Description
[11:0]	RW	12'b0	HST_LNGTH	HST downstream transfer count in bytes.

Host Wait-State Control

Register 24'h380054—HST_WSC

Bits	Type	Default	Name	Description
[31:28]	RW	4'h1	HST_W3W	Wait state control for external write cycles to chip select: HCS[3]#. Length of write cycle = (register value * bclk period)
[27:24]	RW	4'h1	HST_W2W	HCS[2] write cycle.
[23:20]	RW	4'h1	HST_W1W	HCS[1] write cycle.
[19:16]	RW	4'h1	HST_W0W	HCS[0] write cycle.
[15:12]	RW	4'h1	HST_W3R	Wait state control for external read cycles to chip select: HCS[3]#. Length of write cycle = (register value * bclk period)
[11:8]	RW	4'h1	HST_W2R	HCS[2] read cycle.
[7:4]	RW	4'h1	HST_W1R	HCS[1] read cycle.
[3:0]	RW	4'h1	HST_W0R	HCS[0] read cycle.

Host Transfer Control

Register 24'h380058—HST_XFER_CNTL

Bits	Type	Default	Name	Description
[15]	RW	1'b0	Hcs3_cs_hold	HCS[3] chip select hold time (15ns) relative to read or write enable (1 = On, 0 = Off)
[14]	RW	1'b0	Hcs2_cs_hold	HCS[2] chip select hold time
[13]	RW	1'b0	Hcs1_cs_hold	HCS[1] chip select hold time
[12]	RW	1'b0	Hcs0_cs_hold	HCS[0] chip select hold time
[11]	RW	1'b0	Hcs3_ds_polarity	External Data Strobe polarity for HCS[3](1 = positive 0 = negative) Motorola mode only.
[10]	RW	1'b0	Hcs2_ds_polarity	External Data Strobe polarity for HCS[2]
[9]	RW	1'b0	Hcs1_ds_polarity	External Data Strobe polarity for HCS[1]
[8]	RW	1'b0	Hcs0_ds_polarity	External Data Strobe polarity for HCS[0]
[7]	RW	1'b0	Hcs3_xfer_mode	External Transfer mode for HCS[3](we# and re# or R/W# and ds#) (intel(0) or Motorola(1)
[6]	RW	1'b0	Hcs2_xfer_mode	External Transfer mode for HCS[2]
[5]	RW	1'b0	Hcs1_xfer_mode	External Transfer mode for HCS[1]
[4]	RW	1'b0	Hcs0_xfer_mode	External Transfer mode for HCS[0]
[3]	RW	1'b0	Hcs2_sh_extend	External data setup and hold time extend for HCS[3] (0 = 1x bclk period 1 = 2x bclk period)
[2]	RW	1'b0	Hcs2_sh_extend	External setup and hold extend for HCS[2]
[1]	RW	1'b0	Hcs1_sh_extend	External setup and hold extend for HCS[1]
[0]	RW	1'b0	Hcs0_sh_extend	External setup and hold extend for HCS[0]

Host Interface Width

Register 24'h38005C—EXT_INTF_WIDTH

Bits	Type	Default	Name	Description
[3]	RW	1'b0	Ext_intf_width[3]	HCS3: (0): 16-bit (multiplexed), (1): 8-bit
[2]	RW	1'b0	Ext_intf_width[2]	HCS2: (0): 16-bit (multiplexed), (1): 8-bit
[1]	RW	1'b0	Ext_intf_width[1]	HCS1: (0): 16-bit (multiplexed), (1): 8-bit
[0]	RW	1'b0	Ext_intf_width[0]	HCS0: (0): 16-bit (multiplexed), (1): 8-bit

Host Peripheral Handshake

Register 24'h380060—HRDY_HANDSHAKE

Bits	Type	Default	Name	Description
[3]	RW	1'b0	Mstr_handshake[3]	HCS3 HRDY handshake enable bit
[2]	RW	1'b0	Mstr_handshake[2]	HCS2 HRDY handshake enable bit
[1]	RW	1'b0	Mstr_handshake[1]	HCS1 HRDY handshake enable bit
[0]	RW	1'b0	Mstr_handshake[0]	HCS0 HRDY handshake enable bit

Host Multiplexed 16-bit Xfer Parameters

Register 24'h380064—MUX16_PARAM

Bits	Type	Default	Name	Description
[31:28]	RW	4'b0001	HCS3_ale_timing	HCS3 Address Latch Enable timing (register value * bclk period) after HCS goes active
[27:24]	RW	4'b0001	HCS2_ale_timing	HCS2 Address Latch Enable timing
[23:20]	RW	4'b0001	HCS1_ale_timing	HCS1 Address Latch Enable timing
[19:16]	RW	4'b0001	HCS0_ale_timing	HCS0 Address Latch Enable timing
[15:12]	RW	4'b0010	HCS3_addr_cyc	HCS3 Address cycle width (register value * bclk period) setup time not included
[11:8]	RW	4'b0010	HCS2_addr_cyc	HCS2 Address cycle width
[7:4]	RW	4'b0010	HCS1_addr_cyc	HCS1 Address cycle width
[3:0]	RW	4'b0010	HCS0_addr_cyc	HCS0 Address cycle width

Host Chip Select Mode

Register 24'h380068—HCS_MODE_SEL

Bits	Type	Default	Name	Description
[0]	RW	1'b0	HCS_mode_sel	This bit selects between the two possible chip select modes: 0: 2-bit dedicated chip selects. For times when two or fewer devices are connected to the host port. 1: 2-bit encoded chip selects. For times when more than two devices are connected to the host port.

Host Software Reset

Register 24'h38C06C—HOST_SOFT_RST

Bits	Type	Default	Name	Description
[0]	WO	1'b0	HOST_SOFT_RST	Host Software Reset. Writing a 1 to this register triggers a reset of the host logic.

Host Interrupt Mask

Register 24'h200090—HST_INT_MSK

Bits	Type	Default	Name	Description
[19:0]	RW	20'b0	HST_INT_MSK	A value of 1 enables the corresponding interrupt bit location in the HST_INT_STAT register. Unmasking a bit may generate an interrupt immediately due to a previously pending condition. The interrupt remains asserted until the device driver clears or masks the pending request.

Host Interrupt Status

Register 24'h200094—HST_INT_STAT

Bits	Type	Default	Name	Description
[19]	RR	1'b0	PCI_ABORT	Set when the PCI master does a master-abort, or a target responds with a target-abort.
[18]	RR	1'b0	RIP_ERR	Set when a data parity error is detected (parity error response must be set while the master is reading RISC instructions.
[17]	RR	1'b0	PAR_ERR	Set when a parity error is detected on the PCI bus for any of the transactions, R/W, address/data phases, master/ target, regardless of the parity error response bit.
[16]	RR	1'b0	OPC_ERR	Set when the RISC controller detects a reserved/unused opcode in the instruction sequence.
[13]	RR	1'b0	UP_SYNC	Set when number of lines or bytes do not match the upstream host RISC program expectations.
[12]	RR	1'b0	DN_SYNC	Set when number of lines or bytes do not match the downstream host RISC program expectations.
[9]	RR	1'b0	UPF_UF	Set when upstream host FIFO underflow condition is being handled.
[8]	RR	1'b0	DNF_OF	Set when downstream host FIFO overflow condition is being handled.
[5]	RR	1'b0	UP_RISCI2	Set when the IRQ2 bit in a upstream host RISC instruction is set.
[4]	RR	1'b0	DN_RISCI2	Set when the IRQ2 bit in a downstream host RISC instruction is set.
[1]	RR	1'b0	UP_RISCI1	Set when the IRQ1 bit in a upstream host RISC instruction is set.
[0]	RR	1'b0	DN_RISCI1	Set when the IRQ1 bit in a downstream host RISC instruction is set.

Host Interrupt Masked Status

Register 24'h200098—HST_INT_MSTAT

Bits	Type	Default	Name	Description
[19:0]	RO	20'b0	HST_INT_MSTAT	These bits are the logical AND of the corresponding bits in the status and mask registers.

Host Interrupt Set Status

Register 24'h20009C—HST_INT_SSTAT

Bits	Type	Default	Name	Description
[16:0]	WO	17'b0	HST_INT_SSTAT	Writing a 1 to these bits sets the corresponding bits in the status register.

6 Electrical and Mechanical Specifications

6.1 DC Electrical Parameters

The DC electrical parameters are specified in Tables 28 through 30.

Table 28. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
I/O Power Supply	VDDIO	3.0	3.3	3.6	V
Core Power Supply	VDD, VPP	1.71	1.8	1.89	V
PCI I/O High Voltage Clamp Supply	VIO	3.0	—	5.5	V
Input Voltage Low	V_{IL}	–0.5	—	0.8	V
Input Voltage High	V_{IH}	2.0	—	VDDIO+ 0.3	V
Output Voltage Low	V_{OL}	0.0	—	0.4	V
Output Voltage High	V_{OH}	2.4	—	VDDIO	V
MUX1, MUX2, MUX3, and MUX4 Input Range (AC coupling required)	—	0.5	0.8	2.5	V
C_{IN} Amplitude Range (AC coupling required)	—	0.5	0.8	2.5	V
Audio Input Range (AC coupling required)	—	0.1	0.8	2.5	Vp–p
Audio Output Range R_{Load} = 500 Ω	—	—	2	—	Vp–p
Ambient Operating Temperature	TA	0	—	+70	°C

Table 29. Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
VAA (measured to AGND)		VAXTL, VADA, VAACR	—	5.0	V
VDD (measured to GND)		VDD	—	3.0	V
VDDIO I/O Supply		VDDIO	—	5	V
VIO PCI 5V Clamp ref		VIO	—	6	V
Voltage on any Signal Pin(1)	PCI pins	—	AGND – 0.5	VIO +0.5	V
	Non-PCI pins	—	DGND – 0.5	VDDIO + 0.5	V
Analog Input Voltage		—	VAA – 0.5	VAA + 0.5	V
Ambient Operating Temperature		TA	0	+70	°C
Storage Temperature		TS	–65	+150	°C
Junction Temperature		TJ	—	+125	°C
Vapor Phase Soldering (15 seconds)		TVSOL	—	+220	°C

GENERAL NOTES:

1. Stresses above those listed may cause permanent damage to the device. This is a stress rating only, and functional operation at these or any other conditions above those listed in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the power supply voltage by more than +0.5 V or drops below ground by more than +0.5 V can induce destructive latchup.

FOOTNOTES:

(1) These ratings are relative to operating condition power supply voltages.

Table 30. DC Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Digital Inputs					
PCI Inputs					
Input High Voltage (TTL)	V_{IH}	2.0	—	VIO + 0.5	V
Input Low Voltage (TTL)	V_{IL}	–0.5	—	0.8	V
GPIO Input					
Input High Voltage	V_{IH}	2.0	—	VDDIO + 0.5	V
Input Low Voltage	V_{IL}	DGND– 0.5	—	0.8	V
Serial Bus Input					
Input High Voltage	V_{IH}	0.7 * VDDIO	—	VDDIO + 0.5	V
Input Low Voltage	V_{IL}	DGND – 0.5	—	0.3 * VDDIO	V
Digital Outputs					
PCI Outputs					
Output High Voltage (I_{OH} = –2 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}	—	—	0.55	V
GPIO					
Output High Voltage (I_{OH} = –1.2 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 6 mA)	V_{OL}	—	—	0.4	V
Three-State Current	I_{OZ}	—	—	10	µA
Output Capacitance	C_O	—	—	—	pF
Serial Bus Output					
Output Low Voltage (IOL = 3 mA)	V_{OL}	—	—	0.4	V

6.2 AC Electrical Parameters

AC electrical parameters are specified in Tables 31 through 33. Timing diagrams for clock and JTAG are provided in Figures 72 and 73.

Table 31. Clock Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
8 × NTSC Fsc Rate (50 ppm source required)	FS	28.63493	28.63636	28.63779	MHz
XTI Input:					
Cycle Time	1	—	34.92	—	ns
High Time	2	16.6 ± 5%	—	—	ns
Low Time	3	16.6 ± 5%	—	—	ns

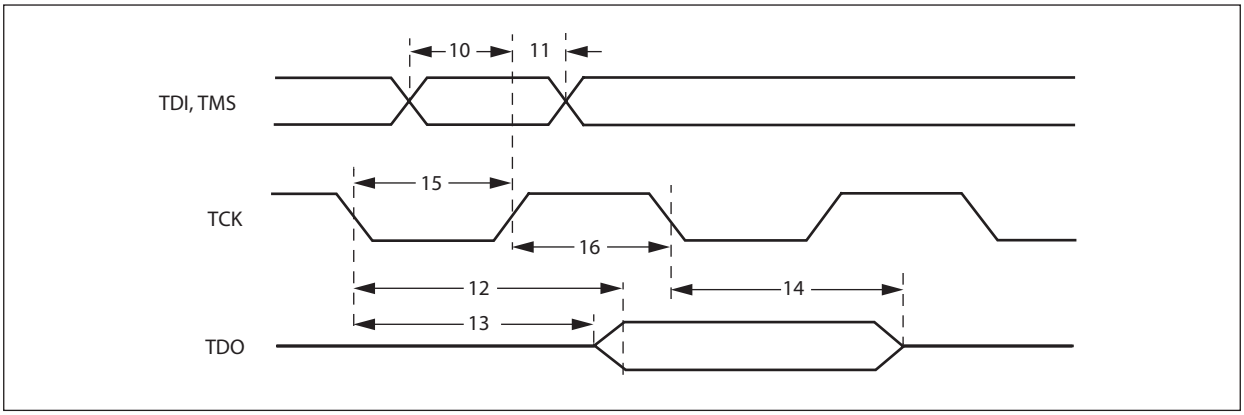
Table 32. Power Supply Current Parameters

Parameter	Symbol	Min	Typ	Max	Units
Core Logic Current: TA = 25 °C, VDD, VDP = 1.8 V	IDD + IPP	—	150	—	mA
I/O Current: TA = 25 °C, VDDIO = 3.3 V	IDDIO	—	60	—	mA
Analog Current: TA = 25 °C, VAA = 3.3 V	IAA	—	200	—	mA

Table 33. JTAG Timing Parameters

Parameter	Symbol	Min	Typ	Max	Units
TMS, TDI setup time	10	—	2	—	ns
TMS, TDI hold time	11	—	2	—	ns
TCK asserted to TDO valid	12	—	15	—	ns
TCK asserted to TDO driven	13	—	14	—	ns
TCK negated to TDO three-stated	14	—	85	—	ns
TCK low time	15	25	—	—	ns
TCK high time	16	25	—	—	ns

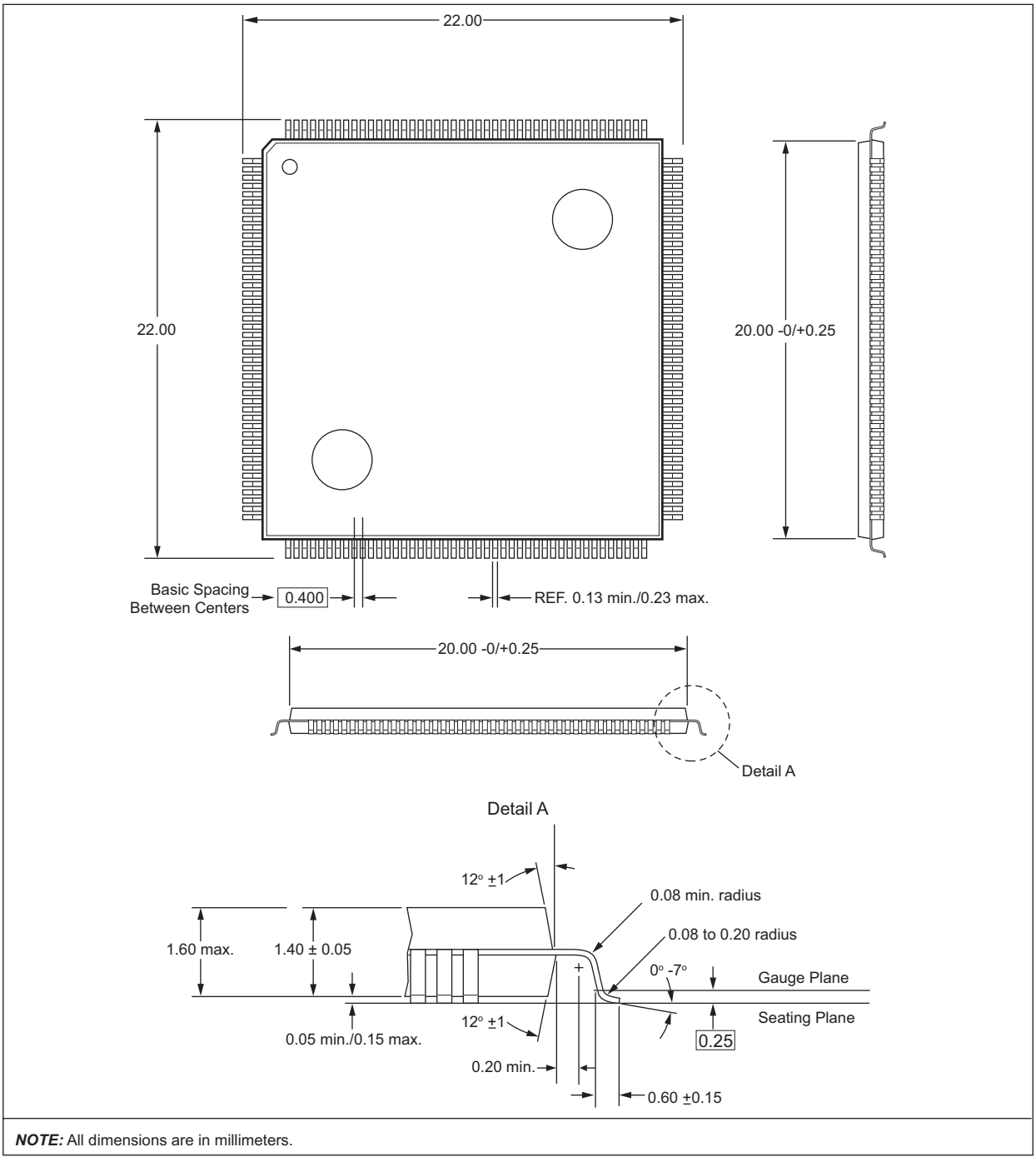
Figure 72. JTAG Timing Diagram



6.3 Package Mechanical Drawing

Figure 73 provides a mechanical drawing of the 176-pin Thin Quad Flat Pack (TQFP) package.

Figure 73. 176-pin TQFP Package Mechanical Drawing



NOTE: All dimensions are in millimeters.

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